AEROSPACE REPORT NO.
TOR-2013-00297

Electrical Design Worst-Case Circuit Analysis: Guidelines and Draft Standard

June 3, 2013

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Electronics Engineering Subdivision
Electronics and Sensor Division

Prepared for:

Space and Missile Systems Center
Air Force Space Command
483 N. Aviation Blvd.
El Segundo, CA 90245-2808

Contract No. FA8802-09-C-0001

Authorized by: Space Systems Group

Developed in conjunction with Government and Industry contributions as part of the U.S. Space Programs Mission Assurance Improvement Workshop.

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Development of the Electrical Design Worst-Case Circuit Analysis Guidelines and Draft Standard resulted from the efforts of Mission Assurance Improvement Workshop (MAIW) topic teams over a two-year period, 2012 and 2013, resulting in a single guidelines document that represents contributions over both years. Significant technical inputs, knowledge sharing, and disclosure of internal guidance documents and command media were provided by members to leverage the industrial base to the greatest extent possible. Special thanks to Cheryl Sakaizawa for her logistical support to the team, which made our meetings run smoothly.

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Executive Summary

This document was produced under the auspices of the Mission Assurance Improvement Workshop during the 2012-2013 year. It is a continuation of the effort begun in the 2011-2012 year. A multi-discipline team was assembled in order to evaluate Worst Case Circuit Analysis (WCCA) best practices and to codify these in a Draft Standard as well as a guidebook. The Draft Standard is written in the form of a compliance standard. From this, selected requirements may be extracted for inclusion in supplier work statements to ensure that the level of WCCA is appropriate for the mission risk level. The Draft Standard may also be used as a starting point for a formal industry standard at some future point.

The Guidebook is intended to provide best practices for performing a successful WCCA, from general principles to detailed guidance at the circuit level. Due to the ambitious nature of this undertaking, the team was not able in 2012 to make the comprehensive guide that was envisioned. Therefore, the MAIW steering committee granted a continuation of the effort for the 2013 year.

The resultant document contains the combined output of the 2012 and 2013 material. The 2012 work was published as Aerospace TOR-2012(8960)-4. There was also a Revision A of that TOR, which was a publically-releasable shortened version of it. This consisted of the main body of the guidebook and the draft standard, omitting the appendices, which were deemed to be export-controlled.

In this 2013 TOR, the main body of the 2012 version of the TOR has remained very much the same, with the exception of section 3.G, “WCCA Statistical Validity.” This section has been augmented with more statistical background and guidance. Appendix A, the Draft Standard, has remained the same. Appendices B through J and L contain new material for 2013. Appendix K contains most of the material from the 2012 TOR that was contained in its appendices.

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1. Introduction to Worst Case Circuit Analysis

A. Purpose

Building electronic systems for high-reliability space applications requires diligent application of the best design practices, use of the highest-reliability parts and materials, proven manufacturing processes, and rigorous testing under environmental conditions that bracket the expected conditions on orbit.

Because space equipment must work reliably and meet specification over the design life, it is also necessary to understand the ways in which variations in the parameters of every part in every circuit could vary over the design life, due to factors including initial tolerance, operating temperature swings, the total dose and dose-rate radiation environment, and aging or drift due to a variety of possible mechanisms.

Worst Case Circuit Analysis (WCCA) is the means by which we determine whether or not circuitry will work as intended given that each constituent part is subject to such variations over life. In WCCA, we aim to prove that, even if all parameters of all parts were to change simultaneously to their most unfavorable values, the circuit would still have a very high probability of meeting its performance requirements over the mission life. Historically, in the military, high-reliability space world, WCCA has been performed during the interval between Preliminary Design Review (PDR) and Critical Design Review (CDR) for a given electronic unit, with the final WCCA report due as a deliverable at CDR. However, this approach lacks visibility and progress monitoring of the WCCA, which can lead to discovery of issues late in the development when there is less time to remedy the problem. Examples of common problems include:

- WCCA activity not begun early enough, not concurrent with design, or not adequately staffed
- WCCA does not reflect as-built hardware
- Incomplete flow of applicable requirements from the unit level to the WCCA
- Omission of analyses that, while critical to successful operation, do not correspond to an explicit requirement for the overall electronic unit, such as phase and gain margin in a power converter
- Omission of interface requirements in the WCCA
- Inadequate parts modeling and correlation
- Inadequate documentation of analyses
- Insufficient independent review of analyses
- No uniform standards for performing WCCA
- Inadequate supporting and correlating test data
- Poor or incomplete SCDs
- Unknown or ill-defined tolerances (especially aging)
- Budget related escapes

Escapes in the WCCA process translate into a higher probability of circuit malfunction in test or on orbit. Thus, a well-executed WCCA is a critical contributor to mission assurance especially given the goal of 100% mission assurance.

The goal of this guidebook, which is being written to complement the draft standard, was also written by this MAIW team and included here as Appendix A, is to provide guidance in all aspects of producing a quality WCCA for any type of electronic equipment. The key to a successful WCCA lies, above all, in the planning, and we present a new paradigm (which has already been implemented on one major program) in which a formal WCCA Plan is presented as a PDR deliverable. This WCCA plan is essentially a mapping from the complete set of requirements to the particular circuit analyses that will show compliance (it is understood that the design will not be finalized at PDR, but the WCCA Plan provides a basis for tracking completion as the design matures). In addition, the WCCA Plan provides other information pertaining to parts characterization, math, and solver tools to be used, how derived requirements will be generated and tracked, and so on.

Another paradigm shift is to provide better feedback and real-time review during the WCCA phase, rather than waiting until CDR for a deliverable that might not meet expectations, as sometimes happens. By conducting a few informal interim tabletop meetings with the customer and independent reviewers while the analysis is unfolding, expectations can be made clearer and misunderstandings avoided.

Although our focus here is on performance WCCA, which establishes whether a circuit meets its performance requirements, we also treat the subject of electrical stress analysis, which is analysis that proves that parts are used in a way consistent with their voltage, current, and power safe-operating levels, with special attention paid to the transient stress analysis. Appendix C contains guidelines for electrical stress analysis. Note that although performance WCCA and stress analysis are often delivered together, they are really independent activities. However, stress analysis should be performed prior to performance WCCA so that suitability of parts can be determined.

B. Relation of WCCA to Other Required Analyses

- Reliability analysis calculates the probability of success of a spacecraft over its design or mission life. It uses established failure rates of parts, takes into account redundancy and cross-strapping provisions in the design. It is the job of the Electrical Stress Analysis to verify that the stress applied to each part is within derated stress ratings. It is the job of the performance WCCA to determine that the probability of circuit variations due to component parameter variations over life and environments is acceptably small.
- Failure Modes and Effects Analysis (FMEA) shows what the system impacts would be for various failure modes in a system. The FMEA seeks to identify Single-Point Failure Modes (SPFMs), that is, single failures that could somehow thwart the intended redundancy in a system, thus causing a total loss of some mission capability. Ideally, an FMEA should be done down to the piece-part level of every circuit, but typically it only extends down to the functional block level. WCCA is substantively different from FMEA, but because the WCCA analysts become so familiar with the detailed operation of every circuit, it behooves them to be on the lookout for component failures that could cause a loss of redundancy (such as components in a cross-strapping circuit), and report any such findings to the FMEA analysts. Conversely, FMEA analysts should help the WCCA analysts determine which circuits are critical.
- Single Event Effects (SEE) analysis is done by the radiation group. Solid-state devices to be used in the design are evaluated as to the rate at which they will experience Single Event Upsets (SEU), Single Event Transients (SET), or other responses to the proton or heavy-ion environment on orbit. The radiation engineer's primary concern is the device's ability to survive single events. However, there are cases where SETs, though not harmful to the device, may result in deleterious circuit-level upsets, which may cause intermittent operation or inflict damage on neighboring circuitry. The WCCA analyst should communicate with the

radiation group to understand device SEE behaviors and ensure that the circuits are designed to ameliorate possible harmful effects at the circuit level, if a device experiences a glitch due to an impinging charged particle. The WCCA analyst must also understand how an SET in one circuit can cause damage or malfunction to neighboring circuits. Modeling of these effects is key to providing a robust design.

- Thermal analysis is performed on electronic equipment to predict the range of temperatures that will be encountered at the unit baseplate, across the surfaces of circuit cards or modules, individual component case temperatures, and junction temperature rise in solid-state components. Because WCCA requires this information to determine temperature-induced parameter variations, WCCA and thermal analysis are thus closely intertwined. Since the thermal analysis of a unit generally lags the circuit design phase, the WCCA analyst typically makes pessimistic temperature assumptions, and only if the circuit does not meet requirements using these assumptions will an analysis need to be refined after the thermal analysis is completed.
- Radiation and life analysis to determine part parameter variations over the life of the part – this flows directly into the WCCA.

It is very important to have good cross-flow of information between these common analytical disciplines during the design and analysis processes, so that assumptions can be understood by all; this gives the highest likelihood that subtle problems can be uncovered.

C. Types of WCCA

The advance of technology has led to more and more sophisticated sensing and processing capabilities for modern satellites. This has had implications for the way that WCCA is done. The following is a summary of the main types of circuits and how WCCA is carried out in this day and age.

Analog Circuitry

Analog circuitry generally refers to low- to moderate- frequency (i.e., lower than what is normally considered "RF") general-purpose electronics used for amplification, filtering, voltage regulation, pulse-width modulation, comparators, and so on. Strictly speaking, sometimes we consider circuits to be analog, even though they may be producing a digital output, such as a discrete transistor driver or a comparator circuit.

Analog WCCA is generally performed using classical circuit theory with lumped parameters. It can be done by writing circuit equations, which is often done for simple circuits of only a few nodes, or circuit simulation software can be used instead. The value of writing out equations is that it gives a deeper understanding of how the circuit works and which parameters have the greatest effect on the output. Simulation can be used for small or large circuits alike, and it is faster, easier, and more accurate than manual analysis, but it does not give the same insight, and there are pitfalls that can result in wrong answers. Simulations must, therefore, be accompanied with a manual approximation analyses to increase circuit function understanding and as a "sanity check" on the simulation results.

Analog circuits often contain a mixture of passive components (resistors, capacitors, inductors, etc.), discrete solid-state devices (such as transistors and diodes), linear integrated circuits (operational amplifiers, comparators, regulators, etc.), or custom analog or mixed-signal Application Specific Integrated Circuits (ASICs). Each type of device has multiple characteristics and parameters that can vary depending on electrical and environmental conditions. Checklists are key to determining which are needed for a particular analysis. A goal of this guidebook is to provide such checklists and other

guidance to assist the analyst and ensure that each analysis includes all the necessary information to ensure a successful design.

Digital Circuitry

Digital systems are comprised of computer processors, memories, peripheral and interface ICs, as well as Field Programmable Gate Arrays (FPGAs) and digital ASICs that have largely supplanted the Small Scale Integration (SSI) and Medium Scale Integration (MSI) devices that were formerly at the core of digital design. Feature sizes of integrated digital devices have shrunk, while operating frequencies have risen. Both the design and analysis of digital systems now requires sophisticated computer tools for logic synthesis and design verification.

WCCA for digital systems primarily seeks to prove that adequate voltage and timing margins exist at the circuit-card and unit levels. In addition, numerous analyses such as stress, transient performance, interface compatibility, and power sequencing, to name a few, must be done over the expected range of voltage, temperature, and environmental conditions to be encountered over life.

As digital systems have become more complex and clock frequencies have risen, signal integrity has become an essential component of WCCA. The physical characteristics of Printed Wiring Boards (PWBs) and backplanes, as well as all connectors and cabling through which digital signals flow, must be carefully modeled and analyzed using specialized Signal Integrity (SI) computer tools. Also, clock skew issues become increasingly dominant in WCCA as frequencies increase.

RF and Microwave Circuitry

Practical (traditional for spacecraft) Radio Frequency (RF) circuits range in frequency from around 10 MHz to 10's of GHz where the electrical circuit interacts with the physical properties of the package and board layouts. Here, the wavelength is small enough that the circuit "feels the effects" and the physical properties of routing and impedance of the path are an important part of the design. Microwave circuits are an extension of the RF circuits and traditionally involve waveguide effects in addition to the above. Microwave circuit frequencies typically range from 1 GHz-100GHz where the wavelengths range from 30 cm to 3 mm. These circuits can involve considerable power, but they can also be very low power where inherent noise is an important consideration.

When the dimensions of the physical infrastructure are on the order of the circuit's operational frequency wavelength, the standard lumped circuit element models break down and do not adequately predict the circuit behavior. Instead distributed circuit elements and transmission-line theory are more useful methods for design and analysis. Open-wire and coaxial transmission lines give way to waveguides and strip line, and lumped-element tuned circuits are replaced by cavity resonators or resonant lines.

Typical spacecraft applications of RF and Microwave circuits are embedded in transmitters and receivers. Transmitters include amplifiers, filters, phase locked loops (PLLs) and/or up/down converters, SSPAs and/or TWTAs. Receivers include low noise amplifiers, filters, PLLs and/or up/down converters. Other "non-traditional" RF circuits include clock distributions for high speed digital circuits.

WCCA for these types of circuits needs to consider both small signal and large signal analysis. Models that include the circuit layouts and packaging used are essential to any RF or Microwave Circuit analysis. The designer must ensure that over all environmental conditions including radiation, temperature, aging, humidity, supply voltage, drive level, packaging, layout and part dimensional and electrical variation, that the devices are never taken beyond a safe operating condition and that the circuit will remain stable. Effects of reflection, polarization, scattering, diffraction, and atmospheric

absorption usually associated with visible light are of practical significance in the study of microwave propagation. The same equations of electromagnetic theory apply at all frequencies.

Tuning is often employed in RF circuits. It is necessary to consider this in the WCCA, but care must be taken with simulation models to ensure that they mimic the physical tuning process.

Power Circuitry

Most electronic units on any spacecraft contain DC-DC converters that convert the main power bus voltage to the voltages required by the unit's internal circuitry. A power converter is itself a self-contained subsystem whose WCCA is mostly analog, along with specialized methods of analysis such as state-space averaging. Also, power WCCA requires detailed knowledge of the operating characteristics of power transistors and rectifiers, as well as magnetic devices.

Power WCCA concerns itself with proving that a converter can provide secondary voltages within a certain tolerance over the range of expected line (input) voltages and load currents, both static levels and dynamic variations, as well as the usual variations in temperature, aging, and radiation environment.

Since DC converters employ negative feedback in order to regulate the secondary voltages, a very important analysis is the stability analysis, which quantifies the stability (amount of phase and gain margin) that will exist under worst-case conditions. Usually this is done via a state-averaged model, as opposed to a time-domain switching model, which is generally only needed for determining open loop performance.

D. Unit-level vs. System- or Interface-level WCCA

Most WCCA is carried out circuit by circuit within a given electronic unit. But every unit has a power interface to the spacecraft power bus, as well as command, telemetry, and data interfaces to other units on the spacecraft. Often, an interface may conform to some standard, such as a 1553 bus, or a Low Voltage Differential Signal (LVDS) interface. The supplier of Unit A provides WCCA to show compliance with the applicable ICD, as does the supplier of Unit B on the other end of the interface. The prime contractor, who has primary responsibility for the overall robustness of the system, must evaluate the detailed performance of the A-B interface to see if any further analysis or test is needed beyond this. At the system level, there may be other phenomena that might cause disruption or damage to an interface. These would include, for example, Electro-Static Discharge (ESD) or transient response to fault events elsewhere in the system, or digital data interfaces with extremely high data rates that may require early risk-reduction testing to confirm viability of the design.

It is recommended that an "Interface Czar" is appointed to be responsible for the successful validation of all data interfaces.

As for the power interface, there are system-level analyses that must be performed to verify compatibility with voltage range and power quality. Also included are system power stability, interface stability, voltage drop analysis, harness stress and heating analyses, and fault protection (fusing) analysis. These are carried out under the auspices of the prime contractor's power group. These are described in detail in AIAA S-122-2007, Electrical Power Systems for Unmanned Spacecraft.

E. The Role of WCCA in Mission Assurance

Consider a circuit that contains some flaw that will cause a malfunction if components vary from their initial values. If WCCA is performed on this circuit as part of the design phase, the flaw will be

found, and the redesign of the circuit will have a minimal impact on cost and schedule. If the WCCA is delayed until sometime after the design phase, the problem may still be found, but now redesign becomes more difficult and costly – engineering drawings and other documents may need to be changed, or the original designer may have moved on to another project, or the lead time for replacement parts may be too long to meet the original schedule.

If a WCCA is not done on the circuit at all, the hardware is built and sent into test. Perhaps the flaw may surface when testing the unit over the qualification temperature range. A test failure results in an investigation, which throws off the schedule and consumes a lot of engineering time. The fix for the problem may now be constrained to parts on hand, addition of white wires to implement a new circuit, or perhaps a decision will be made to accept degraded performance. In any case, the impact will be much greater than if the problem were caught early in the WCCA.

Now suppose the problem is not found until a vehicle-level test, now the box has to be removed from the vehicle, and this may result in a schedule slip for spacecraft test, or possibly even a launch delay. The more time that passes before the flaw surfaces, the more costly it is.

The worst case scenario is when the flaw does not surface until the spacecraft is on orbit. Rather than a temperature related sensitivity, the flaw may only occur after some time in the mission radiation environment. Since both redundancies have the same design, both may eventually fail. If the flaw is one resulting not in mere degradation of some function, but loss of that function, then loss of both redundant sides could mean loss of an important payload or even the entire mission. This translates to not only a tremendous monetary cost, but likely the loss of important space-borne assets.

2. WCCA Programmatics

A. Mission Class

Class A programs are "extremely critical operational systems where all practical measures are taken to ensure mission success. [see Ref. 1 in Appendix F]" Given that it is a "practical measure," comprehensive WCCA is, therefore, mandatory for Class A missions. For Class B, C, or D missions, although a comprehensive WCCA still provides all the benefits or risk reduction discussed above, program budgetary and schedule restrictions may simply not allow it. The challenge becomes how to scale the WCCA to provide the maximum mission assurance benefit given a specific cost allocation. This topic is covered in Appendix 3 of the MAIW Draft Standard (included in this document as Appendix A), "Tailoring Guidance for Class B, C, or D missions."

B. Design Heritage

For new designs of space hardware for Class A programs, nothing less than a complete WCCA will satisfy the WCCA requirement. For heritage equipment, the criteria for deciding whether an existing WCCA is adequate is addressed in Section 2 of the MAIW WCCA Draft Standard (Appendix A) . Those requirements are repeated here.

- WCCA shall be updated whenever any of the following are true:
  - When requirements that were previously verified through WCCA become more demanding.
  - When any circuit is redesigned or modified in such a way as to invalidate elements of the previous WCCA.
  - Whenever parts are substituted, whether for obsolescence or any other reason, and the new part parameter variations are greater than those used in the previous WCCA.
  - When the previous WCCA used lot-dependent performance data, and different lots are used for the new build that exhibit wider parameter variations (either based on the PMP standard or on lot-testing).
  - When part screening, inspection, or observed failure rates indicate a change in characteristic performance or when a part is procured from a different vendor with different performance characteristics or limits.
  - Exceptions: 1) circuits deemed to be non-critical, 2) where large margin exists and it is readily apparent that the change will not jeopardize that margin.
- For heritage designs that are reused, the previous WCCA shall be evaluated to determine the continued validity of each analysis.
- When an earlier WCCA was done using assumptions based on test methods that have been superseded or augmented by more perceptive methods, the WCCA shall be redone (for example, until low dose-rate effects on bipolar technology were discovered, WCCA did not consider them. Today we require ELDRS test results to be factored into WCCA.)
- When equipment designed for a lower class of mission is planned to be used in a higher class (e.g., using a Class C design on a Class A or B mission).

The decision criteria for determining the "continued validity" of a WCCA are as follows.

1. Operating Environment

   If the WCCA for heritage circuits was for an operating environment as severe or more severe than the new intended orbital environment, including operating temperature range, radiation environment, and mission duration, then the original WCCA may still be considered valid. If not, then the original WCCA must be evaluated fully to understand what the impacts of the new, more severe environments would be.

   Extenuating circumstances for accepting the validity of the previous analysis include operational data showing narrower actual temperature swings than those used in the WCCA, and perhaps other flight data that allows some over-conservatism in the original WCCA to be relaxed.

   One common argument made regarding heritage hardware is that substantial anomaly-free operating time on orbit can substitute for a thorough WCCA. While it is true that there is significant confidence gained through successful orbital operation, there are usually not enough units with identical sets of parts to demonstrate high reliability of the design – tantamount to that provided by WCCA – with high confidence.

2. Modifications to Heritage Equipment

   If new circuits are added, or if some existing circuits are modified in a heritage unit, it is acceptable to re-analyze only these circuits. It is generally not necessary to re-analyze circuits that are unchanged, if the new or modified circuits do not have any means of affecting their operation or operating environment.

   The means by which added or changed circuits could affect the old circuits would include such things as different loading on the power sources, added impedances on sensitive nodes, crosstalk or noise via close proximity or shared path impedances, among others.

   The WCCA for a heritage unit with additions or changes would thus consist of full WCCA of the new or changed circuits, plus revised WCCA of those circuits or interfaces affected by the changes. A summary list of the impacts of new or changed circuits should be provided.

C. WCCA Contractual Considerations

Whether a comprehensive WCCA for Class A missions, or something less for Classes B, C, or D, the Statement of Work must call out clearly what is to be done, in order that the contractor or subcontractor can provide accurate cost and staffing estimates and a realistic schedule. Note that until the circuit designs are fairly mature, it may be difficult to anticipate and detail the full scope of the WCCA. The WCCA costing process should take these uncertainties into account.

The MAIW Draft Standard, while not a compliance document, provides language that could be used in Statements of Work and Data Item Descriptions (DIDs). Appendix 3 of that Draft Standard, "Tailoring Guidance for Class B, C, or D missions," can help to formulate criteria.

D. Personnel Requirements

A full unit-level WCCA is an extensive engineering endeavor. A detailed WCCA Plan, in addition to assuring completeness of the analysis effort, also provides an excellent basis for making manpower estimates, as it inherently provides a complete list of analysis tasks and other activities to be done.

Care should be taken in the development of the WCCA scoping/staffing plan and its execution to assure that the WCCA effort is as objective and unbiased as possible. This implies that there should be sufficient resources independent of the primary design organization. While the circuit designers may be involved to a certain extent in the WCCA process, it is recommended, whenever possible, that the WCCA itself be performed by experienced unbiased WCCA analysts. Independent review is essential.

It is recommended that one person be designated as the WCCA "Czar" for the entire spacecraft program, as this will ensure consistent application of requirements, methods, and documentation standards. This person can delegate different subtasks to the designers, coordinators, and peer reviewers, and will also coordinate regularly with the customer and the customer's technical representatives, including the arranging of interim meetings to review the WCCA work in progress.

The unit-level Responsible Design Engineer (RDE) oversees the design and analyses for his or her unit, and also coordinates the interface-level analyses with the prime contractor or other RDEs. The RDE will arrange to obtain specialized analysts when necessary for especially difficult or tricky analyses, and will likewise coordinate any special testing that will be needed to supplement or validate the analyses.

E. In-house versus External Analysis

As in other situations where "make versus buy" decisions are made, there is also a decision to be made regarding WCCA – whether to do the work in-house or to subcontract out the work to an experienced consultant group or analysis house. There are several established companies that specialize in WCCA, and since this is their primary job, they can often do a faster and better job than could the group designing a particular unit, especially a group with inadequate personnel resources for the task.

Here is a list of considerations that can help decide whether subcontracting out the WCCA work makes sense.

- Ability to complete the analysis in the prescribed manner in a timely fashion
- Number and experience levels of in-house personnel capable of doing the job
- Other programs or activities vying for personnel
- Availability or cost of needed analysis tools
- Facilities, equipment, and people available to perform breadboard tests or other special tests
- Cost and schedule considerations
- Access to proven component and circuit models and validated part tolerances
- Access to valid correlation/test data
- Other efficiencies of scale – specialized tools, automatic report generation, etc.

F. Timing of WCCA Activities

Figure 1 depicts the timing of WCCA activities within the program flow.

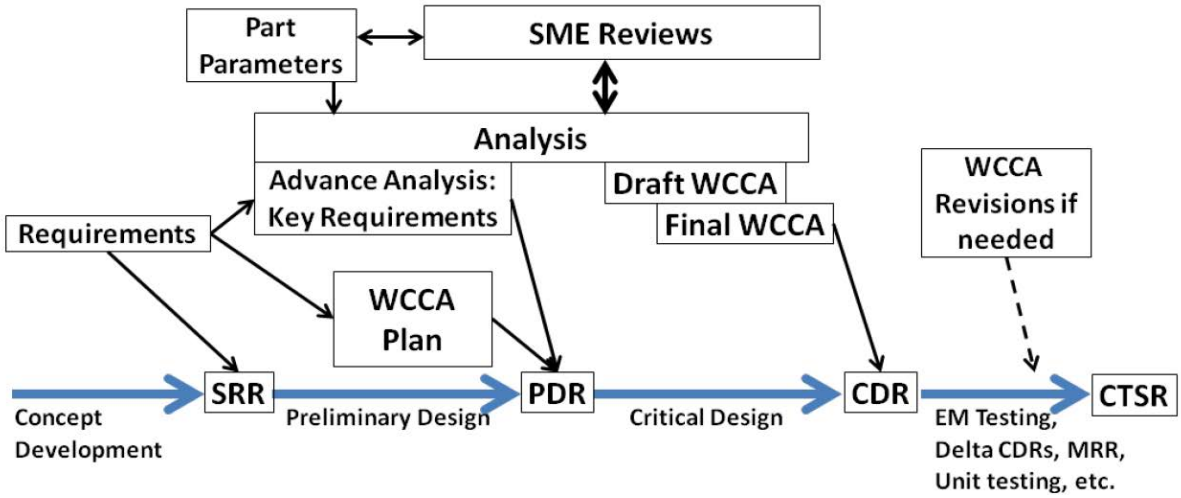

Figure 1. Related analyses: power, thermal, stress.

G. Independent Review

Analysis of electronic circuits requires subject expertise, mathematical skills, skill with simulation tools or mathematical solvers, and the ability to formulate problems and make assumptions or simplifications. No matter what the experience level of the analyst, mistakes or omissions are possible, perhaps inevitable. Even the processes of transcribing equations, entering schematics into a simulator, or other mundane, non-technical aspects of the analysis process are subject to error. Therefore, it is vital to have thorough, comprehensive review of WCCA.

The WCCA process depicted in Figure 1 shows Subject Matter Expert (SME) review both during the analysis process and during the draft report review process. The SMEs can be peers from within the same group or another organization, senior-level experts (so-called “graybeards”), or technical experts working for the customer.

According to the process of Figure 1, analysis begins after SRR and continues all the way to CDR. The first part of the analysis phase includes the writing of the formal WCCA Plan, which is delivered at PDR. The formal WCCA plan should begin as quickly as possible after PDR, as part of the design process. Peer review and informal interim reviews with the customer’s independent reviewers should be done as soon as practicable throughout the process to assess the quality of the ongoing work, identify deficiencies or escapes, or any other aspect of the process. It is anticipated that a minimum of two such meetings should be held for a typical unit under design, more if practicable.

H. Third-Party WCCA for ASICs and Hybrids

When hybrids, ASICs or custom Intellectual Property (IP) circuits from third-party vendors are used in a design, it has been difficult in the past to obtain a full WCCA. The military standard MIL-PRF-38534 for hybrids calls out “Worst Case Circuit Design“(Appendix A, A3.4(e)), but no definition is provided. MIL-PRF-38435 for ASICs does not require a WCCA.

Therefore, when procuring hybrids and ASICs, the Request for Proposal Statement of Work should contain explicit requirements for WCCA to be performed or provided. Appendix E contains detailed guidance for both analog and digital ASICs, as well as for Field Programmable Gate Arrays. Since a

hybrid is composed of discrete parts, its WCCA would follow more or less the same general principles of WCCA discussed in this guidebook. Appendix 2 of the MAIW WCCA Draft Standard, "Detailed Parts Characterization Data," calls out data deliverables for ASICs and Hybrids,

Of course, it is often the case that to perform a WCCA on a hybrid or ASIC, the external circuits, conditions, and loads must be included. Likewise, some system- or unit- level analyses cannot be done without a validated End of Life (EOL) model of a hybrid or ASIC. This problem can be overcome by having vendors provide encrypted, validated models of their devices for inclusion in a higher-level model.

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3. Elements of a Robust WCCA Process

A. WCCA Plan

The WCCA Plan is a formal deliverable document, due at PDR, in which the equipment provider maps out the what/how/when approach to the WCCA process for a unit or other design entity. While this plan may not be fully complete or populated at PDR, all of its elements should be considered. The MAIW WCCA Draft Standard, Section III, contains draft requirements for a WCCA Plan. The basic elements of a WCCA Plan, as given therein, are summarized here:

1. List of applicable documents, such as PMP Standard, SOW, WCA guideline (includes declaring level of analysis and rationale), part derating guidelines, other standards, etc.
2. List of Design Elements (modules or functional blocks)
3. Detailed List of Circuits and Analyses To Be Performed (may be preliminary at PDR, with detail added as designs mature and WCCA proceeds)
4. WCCA Compliance Matrix (WCM)
5. Analysis Methods and Tools
6. Worst-Case Operating Modes and Conditions
7. Personnel Resources
8. Parts Characterization Resources
9. Description of Model Validation Approaches
10. Testing Necessary for WCCA
11. Schedule with Key Milestone Dates

The WCCA Plan simply provides an organized framework for the WCCA process. Much of the work that goes into the plan is work that would have to be done eventually for the final report, even if a formal WCCA Plan were not required.

The most important elements of the WCCA Plan are the list of design elements, the detailed list of circuits and analyses, and the WCCA Compliance Matrix (WCM).

The list of design elements is based on functional decomposition of the unit. The purpose is to show how the unit design will be logically partitioned into modules or functional blocks for WCCA purposes. This partitioning may be by physical boards or modules, or it may be by functions contained on one or more boards. Block diagrams, similar to those which are included in a typical unit specification document, are very useful for visually presenting the intended partitioning scheme.

The list of detailed circuits and analyses are organized by design elements. Every circuit in the unit must be analyzed; it is very important to assure completeness. It is important to assign unique identifiers to each circuit analysis. These will be used in the WCM to track compliance with requirements. For each analysis, there should be a brief description of purpose.

Formal requirements are not the only requirements that must be evaluated in the WCCA. A unit specification specifies *what* the hardware is supposed to do, but it is not always specified exactly *how* it has to do it. *Local* requirements (sometimes called derived requirements) are proposed or created during the circuit design process, or even in the WCCA process itself. A local requirement is

imposed, based on an understanding of the particular implementation of a circuit. The basic principle is, “everything has to work.”

The WCM is a spreadsheet or database that shows every requirement, including all unit-level requirements, interface requirements, relevant system-level requirements, plus local or derived requirements and allocations (i.e., a sub-requirement created by allocating a portion of a higher-level quantitative requirement). The Verification Cross-Reference Matrices (VCRMs) created at SRR for unit specifications, subsystems, interfaces, etc. are a good starting point for determining which requirements need to be flowed into the WCCA. The primary requirements to be verified through WCCA are contained in the VCRM at the unit level. This is usually found in the unit specification. Those whose verification method is “Analysis” are evaluated to determine whether WCCA is the appropriate form of analysis. If they are, they should be listed in the WCCA Plan. Other VCRMs at the system, subsystem, or interface level should be similarly evaluated, with any requirements relevant to the unit-level WCCA included in the WCCA Plan. It is a good idea at this time to double check the other requirements’ types (Test, Inspection, Demonstration) to see if there are any that should actually be addressed by WCCA.

Each requirement in the WCM needs to have an identifier. Formal requirements usually do have these, but local requirements should be assigned identifiers, too. Since these are for WCCA purposes only, they are not formal requirements, and they do not need to be tracked at the system level. The WCM does not have to be part of any official configuration management system. It is just a means of tracking the WCCA activity to completion. The WCM is updated during the WCCA process and is part of the WCCA deliverables.

B. Checklist-Driven WCCA

There are many kinds of circuits and many possible things to analyze. For a given circuit in a given application, decisions must be made as to which of the possible analyses are necessary to perform for the WCCA. An important tool for this decision process is the checklist. Checklists organized by electrical components (resistors, capacitors, etc.) and circuit type can help ensure that nothing important is overlooked. Sample checklists are included in Appendix B.

C. Parts Data

In WCCA, our goal is to compute and validate the nominal performance, and then predict whether circuits will meet requirements given all the deviations from nominal values that the constituent parts could exhibit. This requires knowledge of initial tolerance, temperature dependence, radiation effects, and aging effects of part parameters.

In order to facilitate both the execution of the WCCA activity, as well as the review thereof, it is key to have a systematic means of tracking all the parameter characterization data. Section VI of the WCCA Draft Standard (Appendix A) sets out requirements for a master database. Those requirements are repeated here:

The database shall conform to the following requirements:

1. Organization
    a. The parts database shall be capable of sorting by generic part type (i.e., resistor, capacitor, BJT, power MOSFET, etc.), as well as particular sub-types (e.g., type RM resistors, CLR97 capacitors, etc.). There will also be multiple entries for a single part characteristic, but with different operating points (e.g., transistor beta).

b. A means should be provided to list all usage instances of a particular part type or part number.

2. Contents

   For each particular part type (usually the DSCC part number), the database shall contain the following information:

   a. the parameters relevant to WCCA
   b. initial tolerances of parameters or min/max values
   c. temperature coefficients of parameters
   d. aging or drift tolerances or max values of parameters
   e. radiation tolerances or max values of parameters
   f. references or links to the sources of the data
   g. explanatory notes, where necessary
   h. parameter direction of variation, e.g. biased, random, polarity, unidirectional, etc.

The sources of data that are necessary for WCCA are given in Appendix 2 of the Draft Standard. For Class A programs, the main source of data for most parts will be DSCC data sheets. Data from Radiation Lot Acceptance Testing (RLAT) is also frequently used, as is life test data from vendors that predict variations due to aging. Another good source of guidance on determining EOL part parameter variations is the ESA-ESTEC standard ECSS-Q-60-11A.

Not all parameters can be known at the outset of the WCCA process. It might not be clear which parameters are relevant until equations are written or a Simulation Program with Integrated Circuit Emphasis (SPICE) model built. The specific output function analyzed will drive what characteristics need to be toleranced.

Some parameters are derived quantities based on completed analyses or combinations of more elemental parameters, e.g., switching frequency in a power converter.

It is important to point out that manufacturer's data sheets can usually only be used for WCCA EOL purposes if the minimum and maximum values of parameters are guaranteed for EOL performance, or if RLAT test data is also available. Generally, only space-qualified, rad-hardened part lines would meet the criteria for use in WCCA for high-reliability systems. Of course, BOL and temperature behavior from a non-rad-hard part may generally still be trusted.

Other part types can only be used if adequate testing is performed to determine EOL parameter variations.

Deficiencies in the available parameter data for WCCA should be identified as early as possible so that arrangements to obtain the missing data can be made (e.g., manufacturer inquiries, test programs, etc.).

Oftentimes, RLAT testing to determine EOL parameters will not be completed in time for inclusion in the delivered WCCA. It is therefore a good idea to be pessimistic in the WCCA so that there is a high likelihood that the tested parts will fall within the EOL range assumed for WCCA. Another approach is to "design for WCCA," meaning intentionally selecting the most stable or hardened parts available and using robust design practices so that there is little risk of failing the WCCA. This can eliminate or reduce the need for costly RLAT testing of parts. It will also help extend mission life.

D. Environments

Environments that affect WCCA are as follows:

1. Temperature – Section VI.E of the Draft Standard (Appendix A) calls out use of the qualification or proto-qualification (PQ) temperature range for the WCCA. Some companies use the acceptance (ATP) range instead. Which range to use is a programmatic decision, but technical considerations are as follows.

   Aside from the exposure to thermal cycles in unit-level testing, many units will generally not operate near the hot or cold limits or their ATP range under normal circumstances. So why consider using the qual or PQ range?

   First is the matter of margin. If a WCCA passes using the Qual or PQ range, then there is margin against the ATP range. On the hot side, using qual rather than ATP builds in part temperature margin in the stress analysis and performance margin in the WCCA. On the cold side, the benefit of using the qual range is to provide margin for the cold-start case, when a unit may be at the lower limit of its ATP range. The need for a cold start is rare in space applications; it is more common in terrestrial applications.

   Another level of margin provided by using the qual range is with regard to aging effects. Aging mechanisms are often worse at high temperature, so if the WCCA passes using the assumption of the hot end of the qual range, margin is shown against the ATP range. Of course, local board temperatures and temperature rise due to dissipation in parts in operation must be considered when determining the aging effects.

   In both the environmental testing and in the WCCA, it is important to emulate the operational duty cycles that will be encountered in the mission. A most-stressing Design Reference Mission (DRM) should be developed.

   Lastly, and probably most relevant when there is a PQ unit, is that testing over the PQ temperature range must not cause damage to the unit, since this unit will be flying. A good approach to WCCA when there is a PQ unit is to do the WCCA over both the ATP and PQ temp ranges for critical circuits that might be damaged or cause damage if they malfunction. The ATP WCCA would include all EOL factors, while the PQ WCCA would assume BOL aging and radiation performance, with only the PQ excursions used for temperature. A full EOL WCCA using the ATP temperature range would be used for other circuits, if minor performance degradation when tested over the PQ temp range is acceptably benign. The power converter of any unit should always be analyzed over the PQ range, since malfunction of the converter can easily damage loads.

2. Bus voltage and impedance over frequency – for unregulated buses, ±20% voltage swings are not uncommon. Whatever the range is should be used for analysis of power converters in units as the line variation. Also, EMC requirements such as Conducted Emissions (CE) and Conducted Susceptibility (CS), inrush, outrush, filter stability, as well as all bus transients, including fault-clearing, should be examined by WCCA. The source impedance, including harness and fusing, is a critical driver of power supply performance and must be Included. Changes in the either the bus voltage or source impedance can invalidate most of the WCCA.
3. Radiation environment – the mission radiation environment depends on many factors, including the type of orbit, altitude, and inclination. The total-dose and/or the dose rate radiation environment causes changes to electronic parts that must be accounted for in the WCCA. Single-Event Effects (SEE) can also occur, and while the determination of the frequency of occurrence is done outside of the WCCA process, there must be coordination

with the circuit designers and WCCA analysts to determine that occurrence of SEEs does not result in damage to any parts or too-frequent upsets to operations in circuits.
See also Section VI.A.3 in the Draft Standard (Appendix A), as well as the Radiation Hardness Assurance tutorial in Appendix E for more background and guidance to formulating EOL limits for parts due to radiation effects.

Other worst-case conditions, some of which might be considered "environments," are listed in Section VI of the Draft Standard.

E. Testing Necessary for WCCA

Correlation of circuit models to test data is a key component of WCCA. It is important to validate the nominal model before it is extended to predict EOL behavior. As many analyses as practicable should be correlated with test data. Test waveforms compared to circuit simulation results provide confidence that the circuit was modeled correctly. Other considerations are as follows:

1. Model Verification: Complex models must be verified with test data. Models requiring verification with test data should be identified in the WCCA plan at PDR. Power converter models are a good example of models that must be verified with a brass board using commercial equivalent parts and flight-like magnetics. The brass board test results and model analytical results should conform within acceptable limits in the following areas:

   - phase and gain margin
   - line and load transient response
   - AC line and load response
   - DC regulation
   - EMC emissions
   - EMC susceptibility
   - capacitor ripple current
   - startup and power down transients component stress and power off transients

   Other examples: Motor driver circuits will require analyses similar to power converters, pointing system servo loops and optical encoders, high voltage power supplies, and phase locked loops.

2. Many times part parameters key to an analysis vary widely and are not specified satisfactorily to show compliance with requirements. Special part testing is often required to derive the parameter a range suitable for the WCCA. Examples are timing parameters critical to memory – computer interfaces, ESD and EMC driven noise levels critical to discrete interface circuits and radiation effects on many analog part parameters. In order to derive a valid range "n" parts must be tested, which will result in "n" data points. From the "n" data points the WCCA range is derived using tolerance intervals, which is defined as a range of values for which there is a Y% confidence that X % of the population reside (e.g., 99/90 used in radiation tolerances).
3. There are situations when testing is required because analysis is not practical. Examples are RF circuits that must depend heavily on testing to verify performance will meet requirements. Certain types of resonant power converters are not practical to analyze for stability and other dynamic parameters such as transient line and load regulation. Power on stress and input filter

inrush analyses are very difficult because of saturating filter inductor magnetics. Specific test methods to demonstrate margin must be outlined in the WCCA plan at PDR.

4. Real-life sensitivities to part variations can be measured through use of potentiometers or substitutions of part values from minimum to maximum.
5. Testing of RF circuits is an effective way to see inherent instabilities due to non-linearities and chaotic effects, many of which do not appear in simulations.
6. Testing of high-speed data interfaces using flight-like cables and interconnects, and matching the flight grounding configuration, is an important adjunct to Signal Integrity simulations.

F. WCCA Methodologies

1. Introduction

   Electronic circuits are designed using specific component and parameter values. But components are not ideal; their real values and parameters vary due to manufacturing tolerances and the effects of time and environments. In performing a WCCA, we must consider the effects that initial tolerance, operating temperature, aging, and radiation have on our parts. Every part value or parameter will thus have a range of possible values that it could assume over the mission life. For example, a one kilohm resistor might have an initial tolerance of 1%, variation of ±.15% over temperature, ±2% for aging over life, and ±.02% change due to radiation effects. Thus, in the extreme, the resistor could have any value between 968 and 1032 ohms.

   In circuit analysis, we use component values and other parameters, along with applied excitations and other conditions, to determine some quantity of interest, such as the voltage gain of an amplifier, the output voltage of a power supply, the delay of a digital waveform, etc.

   A good design practice is to "design for WCCA." When designing a circuit, keep in mind the analysis that will need to be done to validate performance. Select robust parts, and design circuits with plenty of margin, to simplify the WCCA process. (As always, there will be trade-offs; selecting a 0.1% resistor may make analysis easier, but may not be worth it as a 0.1% resistor is generally significantly more expensive that a 1% resistor.)

   Let us refer to the quantity of interest in some circuit as X, where X is a function of component parameters, applied excitations, and other conditions. In some cases, it will be possible to write an explicit mathematical expression of the function, while in others, especially for non-linear circuits or those with many components, this may be more difficult or impossible. Nonetheless, let us use the notation,

$$X = f(p_1, p_2, \dots, p_n, E_1, E_2, \dots\ , E_m),$$

   Where the p_i are the parameters and E_j are the applied excitations or other conditions. Since each p and E has its own range of values, determining the possible range of values for the output X can be very difficult. To find the true minimum and maximum values for X is an optimization problem that we generally want no part of unless the function f has few parameters and is amenable to calculus techniques (even then, we would have to be sure that the result would be a global maximum or minimum, not a local one). Instead, we use bracketing techniques to find low and high values for X that encompass the range between the true minimum and the true maximum.

2. Extreme Value Analysis

   One such bracketing technique is called *Extreme Value Analysis* (EVA). In EVA, both the parameters *p* and conditions *E* are set to their most unfavorable values, using some type of defined conservatism to determine what "most unfavorable" means. If the resultant value of *X* lies in an acceptable range of values, then we say that the circuit will work in the worst case.

   EVA requires that the function *f* be expressible as an explicit function of its parameters and conditions in order that we can deduce or calculate which directions of parameter change result in the worst value of *X*. In a simple rational expression, this can often be done by inspection, but for more complicated expressions involving perhaps non-linear functions, determining the worst set of parameters may be extremely difficult. It is not always the case that the worst value of *X* will occur when all the parameters of *f* are at one extreme or another. There are cases where the minimum or maximum value of *X* would occur when one or more *p*'s are somewhere in the middle of their ranges (local minima/maxima vs. absolute minima/maxima).

   If instead of a mathematical expression we use a simulation model of the circuit, there is no *a priori* way to determine how to set parameters to achieve the worst-case. However, a Monte Carlo simulation can be done, randomly varying the parameters for each run and a statistical result can be obtained. Monte Carlo will be discussed in more detail below.

3. Parameter Ranges for WCCA

   In WCCA, as mentioned above, we need to know how component parameters vary – initial tolerance, temperature, aging and radiation. There may be other variations in some cases – these will be lumped under "other."

   These parameters can be either random or biased:

   a. Random: parameter value may increase or decrease unpredictably (for example, a value that may increase or decrease as the component ages)
   b. Biased: parameter value moves in a predictable direction (for example, a value that will increase as temperature increases)

The following are Level 1 (see Figure 3 below) guidelines for incorporating the five constituent parameters (initial, temperature, age, radiation, and other) into circuit parameter (resistors, capacitors, etc.) models.

1. Initial – The beginning of life (BOL) initial tolerances stated are as a percentage of initial value, or absolute min and max limits given in a data sheet, are often absolute measurements based on measurement of each device. Correct application of the manufactures parameter specifications requires understanding of the conditions stated in the data sheet (For example, parameters are often specified over a Vcc and/or temperature range).

2. Temperature – Temperature behavior of a parameter value may be either biased (meaning that the parameter value moves in a predictable direction as temperature change), or random (meaning the parameter value might go in either direction as temperature changes) or a combination of bias and random. Consider the typical resistor. Many resistors have a published temperature coefficient that is random, usually expressed as ± some number of parts per million (ppm). For WCCA purposes, the range of resistance is computed as follows:

R = Ro*(1 + (ppm*1E-6)*(T – 25 C)), where Ro is the nominal resistance, ppm is the specified parts per million per degree C, T is the temperature and 25 C is the temperature at which Ro is specified.

3. Aging – Aging characteristics of some part parameters are determined from life testing, usually at elevated temperature to accelerate the aging process. For other part parameters, tolerances due to aging are provided by program guidelines that are based on life testing of parts constructed with the same technology. Many component parameters are affected very little by aging, while the effects of aging on others have a far greater effect. Aging can be lot-dependent, where some lots might show negligible aging and other lots are significantly affected by aging. An example is a type RM metal film resistors. Some lot tests show aging as low as 0.2% over life, whereas other lots may contain a substantial number whose aging is several percent. MIL-STD-1547B calls out an EOL value of 4% for nominal use, and 7% for "worst-case" use (Condition for worst case: part runs at greater than 50% of its power stress rating). It is best to use conservative assumptions for aging of resistors, as well as other devices, because there are often multiple cumulative aging mechanisms (e.g., stress, temperature, soldering, moisture, shock, etc.).

4. Radiation – Parameter changes in passive components due to the radiation environment are usually benign. For semiconductor devices, radiation effects can be significant. Some types of solid-state components can be obtained from a guaranteed radiation-hardened product line. For these components, the min and max parameter values from the data sheet can be used, provided that the radiation environment is less than program specified percentage Total Dose hardness rated for the part. If this criterion is not met, then Radiation Lot Acceptance Testing (RLAT) may be required. A sample of the parts is irradiated in an appropriate test circuit and the change in some parameter is measured pre- and post- irradiation. From the resulting distribution of the parameter deltas, an appropriate EOL value to be used for WCCA purposes can be derived. Generally, a 2X or greater Radiation Design Margin (R_{DM}) is required. For example, if the total dose level specified for a unit is 10krad over mission life, then the EOL parameter range is determined from the RLAT data for a 20krad dose. In some high-reliability missions, the required R_{DM} may be 3X or higher.

Usually interpretation of radiation or aging test results and determination of the probability distributions of part parameters is difficult. The sigma range (3, 4, 6, etc.) or probability distribution is usually not clearly stated by the manufacturers for the min and max values resulting from the radiation testing.

The test limits given in the DLA "slash" sheets for both discrete semiconductors and for microcircuits may be used as EOL parameters for rad-hard devices. Use the appropriate designation for the radiation levels tested to. See Appendix F for further guidance.

If the max and min values resulting from testing are exceeded in a critical circuit where successful operation depends upon the parameter remaining within limits, the circuit may fail to operate as intended. And if both the primary and redundant circuits use parts from the same lot or process, both could eventually fail, resulting in an important payload failure or even mission failure.

5. Single Event Transients – Note also that other radiation effects may need to be considered in the WCCA. For example, components that exhibit Single Event Transients may need to be analyzed to ensure that circuit damage or a large number of nuisance upsets do not occur. The single event transients are one of many forcing functions included in the level 2 (see below) guidelines.

6. Other Parameters – Other parameters are parameter errors generated by environment such as shock, vibration, thermal shock, humidity and others. These are included in Mil Spec and manufacturer specifications for military grade high reliability parts. The applicable range of these "other" parameters may likely be less than specified, because the applied environment is less than the specified environment. The range to be used in the WCCA shall be determined by the hardware development authority PMP organization. The extracted ranges should be combined by RSS summation to output a composite percent tolerance.

Usually it is very difficult to interpret radiation or aging test results and determine the probability distributions of part parameters. It is not clear what sigma range (3, 4, 6, etc.) or probability distribution the manufacturers is indicating for the stated min/max values. If the values are exceeded in a critical circuit whose successful operation depends strongly on that parameter, the circuit may fail to operate as intended. And if both the primary and redundant circuits use parts from the same lot or process, they could conceivably both eventually fail; thus, an important payload or even the mission itself could fail.

The paper, "Statistical Considerations for Worst-Case Circuit Analysis," in Appendix E, describes in detail some of the statistical hazards involved in determination of EOL limits for WCCA.

Note also that other radiation effects may need to be considered for WCCA. For example, components that exhibit Single Event Transients may need to be analyzed to ensure that occurrence of such does not cause damage in the circuits or result in an inordinate number of nuisance upsets. Such effects can be mitigated through careful design and validated by WCCA.

4. Combining Parameter Variations

For each parameter in our function f, we want to establish a range of values from some minimum to some maximum. For EVA, the method is simple – we take the extremes of the separate ranges for initial tolerance, temperature, aging, and radiation, and sum them to give an overall minimum and maximum for the parameter.

If we do this for every parameter p, and assuming that we know which direction to perturb all of them to obtain the worst-case results, and if we know how to set our excitations and other conditions E to give the worst-case results, then we can go ahead and calculate the minimum and maximum values of X.

If our quantity of interest X meets its requirement using this method, we do not need to go further. EVA is thus fast and effective, and proves that the circuit meets requirements.

However, if the resultant range of X does not meet its requirement, then employing Root-Sum-Square (RSS) techniques or Monte Carlo analysis is permitted, as long as care is taken to ensure that the results meet the required confidence interval with an appropriate confidence level.

One thing to watch out for in using parameters in an analysis is the possibility of impossible conditions. An example of this is a parameter for which min and max values over life have been calculated. If that parameter is used in multiple places within an analysis, one should not assume min in one place and max in another. The parameter can only be one value at a time. One should always take care to assess the circuit equations for situations like this. Similarly, for parameter minima and maxima based on baseplate temperature, applied voltage, and other applied conditions, one must remember that these conditions, if they are global to the circuit

under analysis, can be only one value at a time. Although impossible conditions can sometimes be intentionally assumed as the worst-worst case, they can easily cause the circuit to fail its requirements; if the impossible condition is unintentionally applied, it can result in needless effort to either redesign a circuit, or track down the impossible condition, which may be subtle.

a. EVA Parameter Variations

To determine the range that a parameter may assume, we use the information we have for the initial tolerance, temperature, aging, and radiation behavior of the part. We calculate the greatest positive and negative deltas of each using algebraic summation of the tolerances.

b. Root Sum Square Parameter Variations

EVA is a very conservative methodology. The reason for using it is that it is a good first pass for a circuit. If the circuit passes using EVA, no further work is needed, and one can say that confidence in the circuit is extremely high. When a circuit fails WCCA using EVA, RSS may be applied at the parameter level or at the circuit level. It is recommended that a spreadsheet be used to calculate both EVA and RSS results simultaneously; in case EVA does not pass, the RSS will already be done.

To calculate RSS parameter variations, the following equations are used:

$$WCmin = Nominal - \sum Negative\ Biases - \sqrt{\sum (Random\ Terms)^2}$$

$$WCmax = Nominal + \sum Positive\ Biases + \sqrt{\sum (Random\ Terms)^2}$$

To apply this to our four conditions of initial tolerance, temperature, radiation, and aging, we must be certain of the direction of variation, as well as possible correlations between terms. It is only correct to RSS terms if they are random.

The statistical justifications for using RSS are discussed in Section G below, and in Appendix L.

5. Using Parameters in Circuit Equations or Simulations

Once we have determined worst-case min and max ranges for our part parameters, we move on to the issue of how to use them in analysis. Remember, we have designated a general circuit quantity of interest by our function

$$X = f(p_1, p_2, \dots, p_n, E_1, E_2, \dots\ , E_m).$$

Remember, we have already determined the minimum and maximum worst-case parameter variations; the problem now is to use those to determine the minimum and maximum values of *X*. There are three basic methods that can be used here: EVA Analysis, Sensitivity Analysis, or Monte Carlo (MC) Analysis. These will be discussed shortly.

It is worth emphasizing here that our problem of determining the EOL range for *X* is a two-step process, the first at the parameter level, and the second at the circuit level. Both steps could be either EVA or RSS, or in the case of the circuit output *X*, Monte Carlo (it is

conceivable that MC could be used to combine parameter variations, but this is never done in practice). There is also, in some cases, a third level. This would be when two or more circuits contribute to some overall value, such as a chain of amplifiers. The minimum and maximum gain of each stage is determined by WCCA, based on parameter variations, and then the overall gain is found based on the minima and maxima of all the stages. This too could be either EVA or RSS.

a. EVA at the Circuit Level

In this method, we must be able to express the quantity of interest *X* as an explicit function of the parameters and applied excitations and other conditions. Sometimes, for simple circuits, this can be done in a straightforward manner, using a standard circuit theory approach. If there are multiple parameters and conditions, though, it becomes more difficult to formulate the expressions, and there is more possibility of errors creeping into the process. When circuit equations are written, it is important to validate them either by peer review, circuit simulation, or breadboard testing. Assuming that we have a valid explicit expression for our function *X*, we then have to decide which direction to perturb our parameters to give the worst-case range for *X*. A simple example is the voltage divider, where the "*X*" we want is the output voltage Vx.

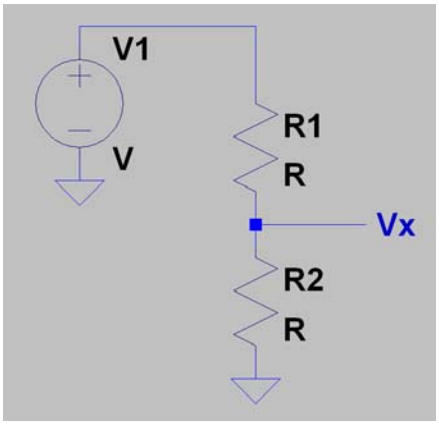

Figure 2. Simple voltage divider.

The equation for Vx is very simple: Vx = V1*(R2/(R1+R2)). From this, we want to derive Vxmin and Vx max, the extremes of our EVA range. For V1, we need to know, possibly from a specification for a power supply, the spec limits. This might be something like ±5%, for example. It is easy to see from the equation that Vx will be minimum when V1 is minimum, and similarly for the maximum. To see which whether R1 and R2 should be set to min or max is more difficult to see by inspection. But if we invert the equation, we have 1/Vx = (1/V1)(1 + R1/R2). From this it is easy to see that Vx is a min when 1/Vx is a max, which occurs for R1 is set at its minimum and R2 is set as its maximum.

Now, if this voltage divider feeds some circuit that provides loading, the equation for Vx will have more terms and it may not be so straightforward to determine whether part values and other parameters should be set to their minimum or maximum values. It is critical that we know how each value should be set to give the worst-case value of Vx.

b. Sensitivity Analysis

When it is difficult or impossible to tell by inspection how to determine the most unfavorable combination of circuit parameters, we may use sensitivity analysis. In this method, we take

the partial derivatives of the desired circuit response, at some operating point, with respect to each parameter (and possibly for certain applied conditions, such as temperature). These are the sensitivities of the circuit. The sensitivities should be checked for monotonicity when this is not readily apparent. If not monotonic over the perturbation range, then the circuit maximum or minimum response might occur for some intermediate parameter value, not its min or max. Strictly speaking mathematically, the sensitivity method is only valid for infinitesimal variations about an operating point. The way it is used for WCCA, our perturbations are finite deviations from a nominal value; the larger these deviations are, the less valid the approach becomes, especially if deviations move us considerably away from our operating point into a different point where the sensitivities may be different or worse, change signs. Therefore, extra care should be taken when dealing with large perturbations.

The product of a parameter sensitivity with the difference between the nominal value and the min or max equals the *differential* of the output response due to the contribution of the parameter. Using our previous notation, we arrive at the minimum and maximum differentials of X due to a parameter p_i,

$$dX_{p_{imin\ or\ max}} = \frac{\partial X}{\partial p_i} * (p_{i\ nom} - p_{imin\ ormax})$$

So for n parameters, we would end up with n differentials. We might also need to calculate differentials for one or more of the applied excitations or conditions, but for simplicity, we limit the discussion to the parameters p_i. We establish the convention that $dX_{p\ I\ min}$ is a negative number, and that $dX_{p\ I\ max}$ is a positive number, such that when we sum them later, we can find the min and max values of X.

Having the differentials calculated, we find the parameters that have the most impact to the WCCA. If circuit modifications are required, we address these components first. We will also find that some are negligible compared to the others, and if so, these may be neglected.

The sensitivities, which are the partial derivatives, have ± signs as well as magnitude, corresponding to the direction of slope of X due to a positive perturbation of p_i. It is essential to use the correct sign in the calculation of the differential. It is also critical to determine whether to use $p_{i\ min}$ or $p_{i\ max}$. If calculating $dX_{i\ min}$ (which will be a negative quantity*)* and the sign of the sensitivity is negative, then we will use $p_{i\ min}$ in the expression above. If the sensitivity is positive, then we use $p_{i\ max}$. If calculating $dX_{i\ max}$ (which will be a positive quantity*)* and the sign of the sensitivity is negative, then we will use $p_{i\ max}$ in the expression above. If the sensitivity is positive, then we use $p_{i\ min}$.

There are two ways to combine all the differentials due to the parameter variations, and create the *total differential* of X, which is our goal. This can be done by EVA or RSS. First we discuss the EVA method. Our goal is to determine X_{min} and X_{max}, which are the upper and lower bounds of the EOL range of our quantity of interest (in the voltage divider example, this was Vx). To find the total differential, we simply sum our differentials for the min or max cases, and add them to the nominal value of X:

$$X_{min} = X_{nom} + \sum_{i=1}^{n} dX_{i\ min}$$

$$X_{max} = X_{nom} + \sum_{i=1}^{n} dX_{i\ max}$$

Because we have selected our parameters terms to ensure that all the $dX_{i\,min}$ are negative and all the $dX_{i\,max}$ terms are positive, we can see that this equations will indeed give the min and max values of X. X_{min} and X_{max} are the worst-case result for the circuit, which can be compared against the specification limits or other requirement. If X_{min} and X_{max} lie between the required limits, the circuit passes EVA; if not, then it fails EVA.

If a circuit fails EVA, then RSS may be used. Section V.E.1 of the Draft Standard (Appendix 1) calls out that use of RSS requires three or more terms, that is, n >2 in our notation. The reason for this restriction is that unless it can be shown conclusively that two variables have normal distributions and are uncorrelated, it is risky to RSS them. With three or more variables, the Central Limit Theorem comes into play, and the risk is lower.

The formulas to use for the RSS sensitivity technique are as follows:

$$X_{min} = X_{nom} - \sqrt{\sum_{i=1}^{n} (dX_{i\,min})^2}$$

$$X_{max} = X_{nom} + \sqrt{\sum_{i=1}^{n} (dX_{i\,max})^2}$$

Since all the dX_i are squared, we must subtract rather than add the terms for $X_{min.}$

Manual sensitivity analysis is usually limited to fairly simple circuits that can be written as a straightforward mathematical expression such that the partial derivatives can be readily determined. When this is not the case, mathematical software packages such as Mathcad are often used. Mathcad allows for more complex expressions to be written, and there are functions that can calculate the partial derivatives of these expressions at a specific operating point.

There is a drawback to using these complex expressions, however, and that is loss of reviewability. How can one be sure that the expressions are correct? The analyst has to enter the circuit expressions piece by piece in order to build up the more complex expressions. There is a very real possibility of error due to incorrect entry on the part of the analyst. As the software combines simple expressions into more complex ones, these errors will be masked. It is, therefore, advisable in the build-up of circuit equations into more complex ones, that the analyst double check the work and also have another engineer double check it. Test cases should be run and compared against bench test or circuit simulation results. By using two independent means of analyzing the circuit, much confidence in the validity of the results is obtained.

Often it is much easier, faster, and less error-prone to use a circuit simulator to determine the sensitivities. DC sensitivity analysis is built into the SPICE language, and most commercial software based on SPICE can be used. The circuit is built with nominal part values and other parameters (which may be explicit or implicitly built into device models). A DC analysis is run, and then the simulator determines sensitivities at the resultant DC operating point. The resultant sensitivities can then be used in either the EVA or RSS equations shown above. It is always prudent to cross-check simulation model results with an alternate method before executing the WCCA with the simulation.

The statistical validity of the RSS technique is explored at length in Appendix L.

c. Monte Carlo (MC) Analysis

As personal computers have become faster and faster, circuit simulations can be done in a tiny fraction of the time it took ten to twenty years ago. This makes Monte Carlo (MC) simulation a more attractive option for WCCA than it was previously.

To run a WCCA using MC, we need to do the following:

- Enter the circuit into the simulation software using netlist or schematic capture
- Specify the range for the part values, parameters, and relevant applied excitations or conditions
- Determine which probability distribution types to use, if available
- Determine the number of runs that will be needed to show the required level of statistical certainty in the results
- Run the simulation, and analyze the resulting data to determine mean and standard deviation of the response, then apply appropriate multiplier to achieve worst-case statistical confidence requirements. The methods for this are discussed at length in Appendix L.

Schematic capture is generally used for circuit entry, but it can be easier to work with a SPICE (or other circuit simulator software) netlist directly to modify device models and set up the simulation parameters (this depends on the particular SPICE implementation). It can be tricky to set up the model to vary some parameters for a MC simulation. For example, the base-emitter capacitance in a BJT is not set directly. One must alter the forward transit time. Sometimes it is easier to create equivalent subcircuits instead of using the detailed device model (especially for setting the Vos, Ios, and Ib for an op amp or comparator – it is sometimes easier to add the appropriate voltage and current sources to an ideal op amp model than to change internal parameters). It depends on what the analysis is trying to prove and the level of device fidelity that is needed. The details of how to enter a probability distribution for a part depends on the particular SPICE implementation – see vendor documentation. There are differences from vendor to vendor. For example, some products allow entry of Gaussian distributions, including tails, whereas others truncate the distribution at the three-sigma points. These subtleties can detract from the validity of the result, so caution and sound statistical awareness should be exercised. Examples of Monte Carlo analysis using PSpice are provided in Appendix L.

A Monte Carlo simulation usually produces a histogram showing the spread of output values over a number of runs. This histogram often looks like a Gaussian "bell" curve, and the simulator usually gives the mean and standard deviation. If not, the data may be imported into a spreadsheet or other software to determine these values. The mean and standard deviation produced by the simulation are not the final result. One must apply statistics to determine what multiplier to apply to the standard deviation to achieve the required probability of success. Two methods can be used for this: Predition Intervals (PI) and Tolerance Intervals (TI). These are discussed below and in Appendix L.

It has been suggested that assigning uniform distributions to parameters rather than normal distributions helps reduce the number of runs needed for MC simulation, because doing so makes it more likely that the parameter end-points will be used in the simulation. Indeed, with a very large number of runs using uniform distributions, the results can be thought of as a kind of quasi-EVA result, which could at times be a useful alternative to true EVA. This topic is discussed in Appendix L.

d. Combining Multiple Circuit Outputs

Besides the parameter variations and the circuit variations, there is another possible level of WCCA, and that is when multiple circuits are combined. A simple case would be three

voltage reference circuits (not necessarily identical) put into series for some reason, and we wish to find the limits for the sum of the three. Assuming that each circuit can be considered standalone and we do not have to worry about interactions between circuits due to loading or other effects, then the nominal total voltage is simply the sum of the three nominal voltages. The EVA extremes of the total output would be the sums of the positive and negative deltas added to the nominal total voltage. The deltas could also be RSS'ed and summed/differenced with the nominal total voltage to give the RSS overall deviations.

The following diagram, from Appendix L, illustrates the three levels of WCCA: parameter, circuit, and multiple-circuit.

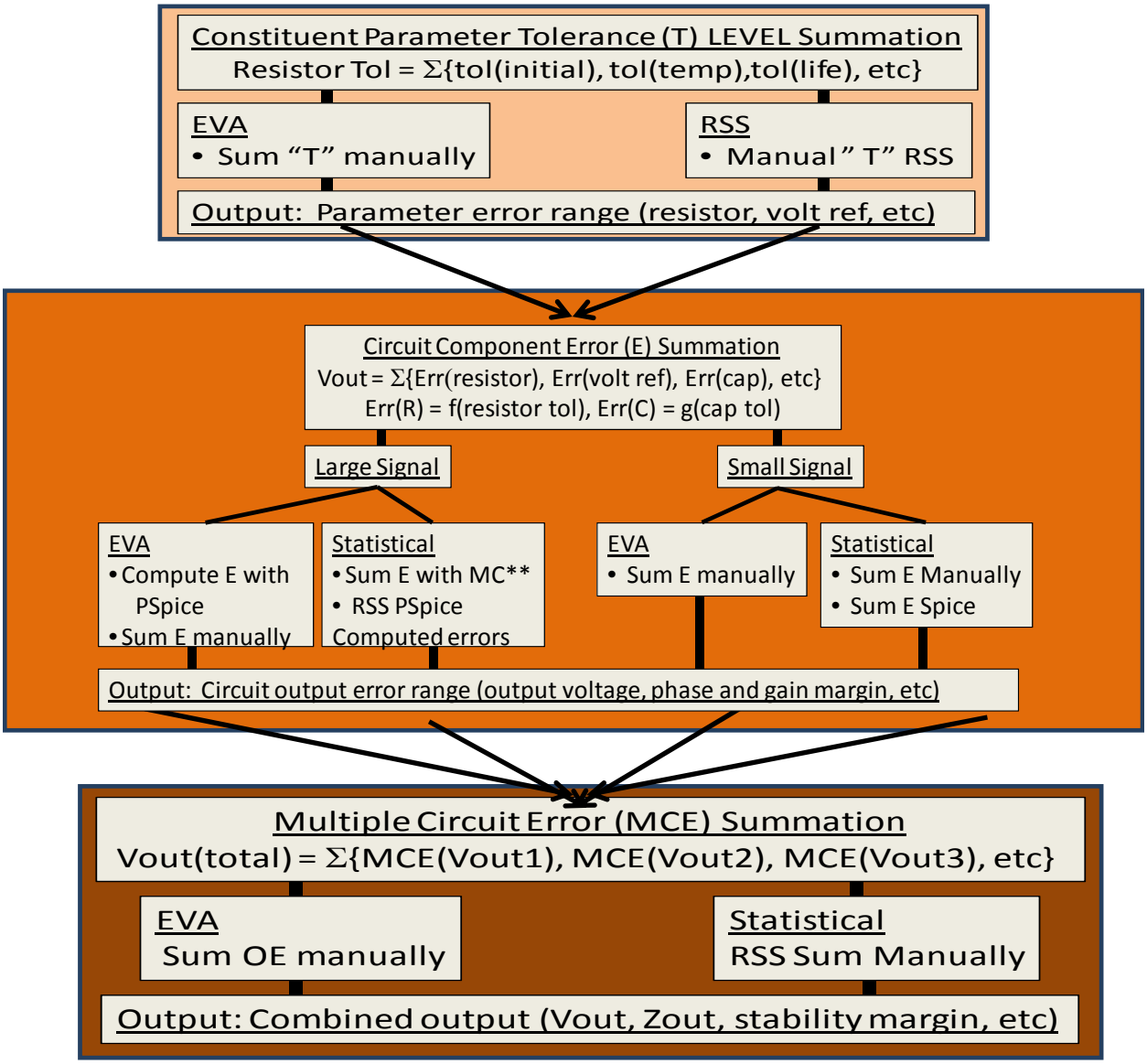

Figure 3. The three levels of WCCA.

Level 1 addresses the constituent parameters, which are the individual constituent parameters (initial, temperature, age, radiation and other) that combine to provide the circuit component parameters such as resistors, capacitors, and voltage references.

Level 2 addresses circuit components which combine to provide the circuit level parameters such as voltages, currents, RF signal strength in dB and others.

Level 3 addresses circuit outputs which combine to provide the larger scale circuit outputs for black boxes or even subsystems.

Each level can be thought of as an integration node, where the level 1 outputs integrate into level 2 and the level 2 outputs integrated into level 3. EVA and RSS methods are addressed for each level of analysis.

G. Statistical Methods for WCCA

The goal of this section is to provide guidelines for the application of statistics to WCCA. The goal includes establishing the role of statistics in WCCA and how statistical analysis can be used to ensure acceptable "WCCA Reliability." The term "WCCA Reliability" applies because the probability of a circuit output being within specified limits can be thought of as the reliability of the circuit staying within limits. Note: If the circuit output does not stay within specified limits, a system failure may result.

This section of the WCCA guideline document addresses the application of EVA and statistics to the small signal and large signal methods of summing error sources. Section F addresses EVA and RSS methods recommended for WCCA and Section G provides additional information with an emphasis on the application of statistics. Appendix L addresses more RSS and EVA detail procedures and also presents WCCA examples using RSS and EVA methods. Much of Section G and Appendix L focus is on statistics, because addressing the probability of exceeding RSS limits is a more complex process compared to the simpler EVA process.

Although the majority of the discussion is related to RSS, the preferred method of error summation is EVA and not RSS. RSS should be used with care if the EVA analysis does not yield results that meet the performance requirements.

RSS has had a long history of application in WCCA and has been very reliable in that the probability of exceeding the RSS limits is very low and in the experience of most designers, RSS limits have never been exceeded. The question addressed herein is: Why is the probability of exceeding RSS limits so low? The following presents an explanation for the low probability of exceedance based upon statistical analysis.

Section G addresses the probability of staying within RSS limits that meets some acceptable level. The circuit output variation is based on part parameter (resistors, capacitors, voltage references, etc.) tolerances and each part parameter variation breaks down into constituent parameters (initial, life, radiation, temperature, and other). Each constituent parameter (CP) has a statistical distribution, which is discussed and estimated in Section G. The part parameter limits and associated distributions are then incorporated into the circuit models used to derive the 3 sigma circuit range of operation. (Output voltages, output currents, output power, component power, system gain and others)

Several methods of RSS and probability calculation are presented in Section G and Appendix L, which are just a few of several acceptable methods. The objective of all the statistical methods presented in Section G and Appendix L is to determine the range of an output parameter, Vo, for which the probability of exceeding Vo is less than .0027. .0027 is equivalent to the two-sided normal distribution 3 sigma limits, diagramed in Figure 4. This statement in equation form:

1.) $Vo(bias) - Vo(RSS) < Vo < Vo(Bias) + Vo(RSS)$

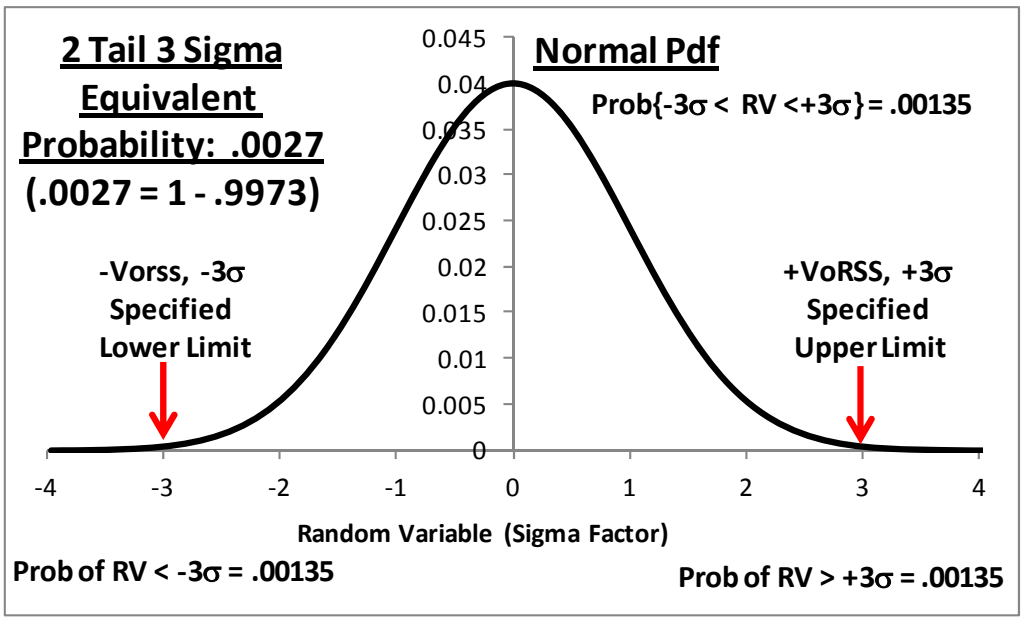

Figure 4. 3 Sigma normal definition.

The probability distributions associated with the CPs (Initial, temperature, radiation, life, and other tolerances) are estimated from general knowledge gained in past experience and are not rigorous. As a result, there is some uncertainty associated with the resulting Vo range of limits. To compensate for this uncertainty and to decrease the chance of the equation 1 limits being deficient (too small), the guideline to follow introduces a constant termed Sigma Factor (SF) that enables the probability of exceeding the RSS limits to be decreased. Equation 2 shows how SF is applied to equation 1.

1.) $Vo(bias) - SF*Vo(RSS) < Vo < Vo(bias) + SF*Vo(RSS)$

SF is a constant, generally between 1.0 and 1.2. As an example, if SF = 1.2, the probability of exceeding the equation 2 range relative to exceeding the equation 1 range is decreased by a factor of 4. Guidelines for applying the SF factor are included later in this section and Appendix L Sub-appendix A.

First, some definitions of what it means to "pass WCCA" are in order and how sigma factors can be applied to ensure "passing WCCA" is accomplished. Consider a power supply whose output voltage is specified to be 15VDC +/-5% (in numerical terms, 14.25V to 15.75V). In this case, there is a firm numerical requirement given in the power supply's specification. The WCCA goal is to show the requirement can be met at EOL with an acceptable probability, which has been established to be 99.73% (corresponding to the three-sigma point on a normal distribution).

As an example of the WCCA process, two analyses are performed for a power supply (using a SPICE model) and the results summarized in the order performed:

Trial 1: Level 1 (parts) EVA and 2 Level (circuit) EVA – results: 14.02 to 15.98V FAIL

Trial 2: Level 1 (parts) EVA, Level 2 (circuit) RSS – results: 14.36 to 15.62 PASS

Note that in trial 2, the constituent parameters (initial, temperature, life, radiation, etc.) are combined using a direct EVA sum and the component parameters (resistors, capacitors, and inductors, etc.) are combined by an RSS summation.

These results are also displayed in Figure 5 and compared to the normal distribution:

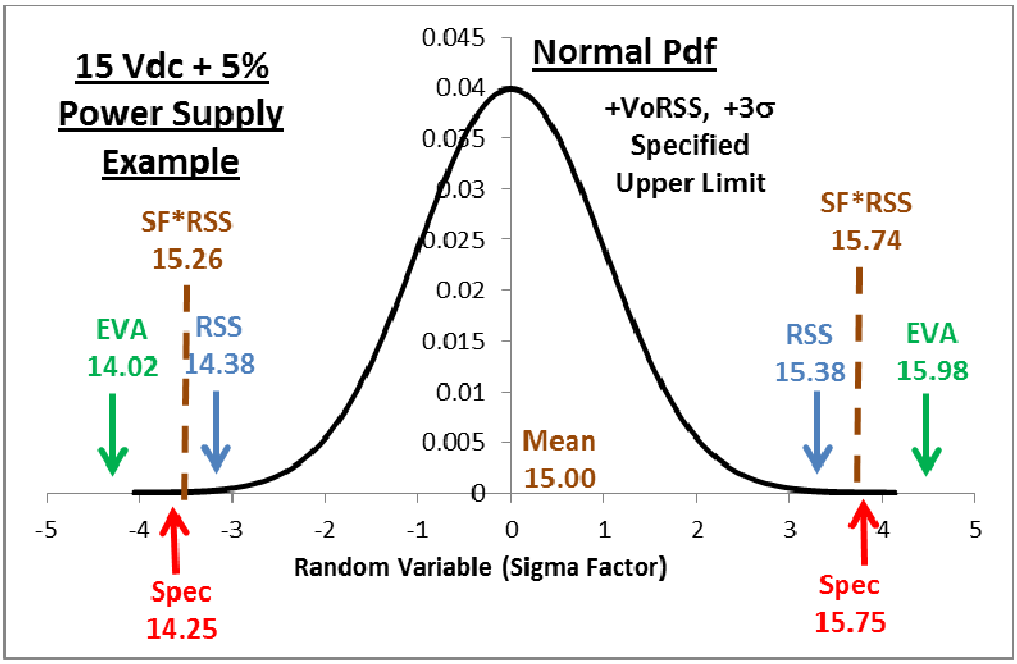

Figure 5. EVA-EVA and EVA-RSS circuit output compared to spec requirements and normal curve.

Using EVA-EVA gives a result that is greater than 4 sigma. Using EVA-RSS gives a result that is greater than 3-sigma, and because the results lie within the specified performance interval, the circuit meets requirements.

The example can be extended to sigma factors discussed in the overview, which is a compromise between and RSS and EVA. If EVA-RSS is needed to "pass WCCA", but there is too much uncertainty in the RSS calculation, then the RSS portion of the limits can be multiplied by a sigma factor to reduce risk. As an example, if the Sigma factor is 1.2, the RSS limit increases to from 15.38 volts to 15.744 volts and the probability of exceeding the RSS*SF limits is reduced by a factor of 7.8. The limits are still within spec and the risk is decreased by a significant factor.

Consider another circuit, a bipolar transistor drive, that must be capable of pulling down the input of some other device below .5 Volts. Here there is no specification requirement to be met, only the requirement that there has to be greater than a 99.73% probability that the circuit will work at EOL.

Guidelines for Combining Constituent Parameters Using EVA and Statistical Methods:

The two methods addressed for combining constituent parameters are extreme value (EVA) and root sum squared (RSS).

1.) EVA is the simple addition of the constituent parameters (CP) listed in Table 1. The level 1 outputs are the part parameters listed in Table 2.

2.) RSS adds the average value part of the CPs to the RSS part of the CPs. Biased variables still need to be simply added. This method more realistically predicts the actual performance of the circuit, but can be more difficult to apply.

Table 1. Constituent Parameter (CP) Tolerances

Notation	Description
Ti	Initial tolerance (%)
Tt	Temperature tolerance (%)
Ta	Aging tolerance (%)
Tr	Radiation tolerance (%)
To	Other (%) (Examples: soldering heat, shock, vibration, thermal cycling, etc)

Table 2. The More Common P Parameters (P)

Notation	Description (units)
R	Resistance (ohms)
C	Capacitance (farads)
L	Inductance (Henries)
Vref	Voltage reference (Volts)
E	Voltage Gain Amplifier
G	Trans-conductance Gain (mhos)
F	Current Gain Amplifier

One of the goals of the Level 1 guideline that derives part parameters is to perform the necessary analysis to ensure the probability of a parameter exceeding its RSS limits is acceptable given the part parameter information available. Determining the probability of exceeding the RSS limits of the outputs at all three levels is based on statistical distributions of the part parameters. However, for very nearly all part parameters, very little data is available to derive statistical distributions.

Acquiring part parameter probability distributions to the extent necessary to satisfactorily correlate probabilities and RSS limits is not practical for the following reasons:

- CP distribution data for each part and from each manufacturer is required.
- Within each manufacturer, data is needed for each lot date code (LDC).
- There are also cases, where parts from several LDCs and/or suppliers are mixed together, possibly creating multi nodal or other non standard distributions.
- The Spice Monte Carlo simulator only accepts one probability distribution for all parameters in a single simulation run. As a result, even if individual part distribution were available, most of the data could not be used in the simulation.
- No hardware development program can tolerate the cost of the added part testing to derive the necessary part distribution data.

Because there is no hope in actually deriving or using the actual part statistical distributions, the question becomes: What is the best that can be done to derive the probability of exceeding the RSS limits?

CP probability estimates can be derived with two ground rules, which will be discussed in detail in the following:

Ground Rule 1: Each CP distribution can be bounded by a normal distribution function.

Ground Rule 2: The manufacturer's specified limits can be placed at the two tail 3 sigma points.

With these two ground rules, standard normal distribution (also known as Gaussian distribution) based statistical methods can be applied.

The five most common constituent parameters (CP) are listed below. No additional statistical distributions are introduced in the levels 1 (part parameters), 2 (circuit parameters) or 3 (multiple circuit output parameters) discussions. The constituent parameters combine to result in the "P" parameter, which are input to the circuit analysis.

Acceptable Probability for a CP and Part Parameter Exceeding WCCA Limits: The acceptable probability for a constituent parameter or part parameter to exceed specification or WCCA limits is 3 sigma normal. This means the probability of one of these parameters exceeding the limits calculated in the RSS analyses is less than 0.0027 (= 1 - .9973), which is equal to the probability of exceeding the normal distribution probability of being outside $\pm$ 3 sigma. Figure 1 presents a diagram of the relationship between 3 sigma and P = .0027.

Refer to Appendix L Sub- Appendix Section 2.1.1 for additional information pertaining to the 3 sigma success criteria.

a. EVA Constituent Parameters

The parameters can be summed as shown in the following equations:

$$3.)\ P = Po * (1\ +/-\ (Ti + Tt + Ta + Tr + To)/100\%)$$

Po is the nominal "P" parameter value (Ro, Co etc).

The T terms are the tolerances of different constituent parameters, listed in Appendix L, Subappendix A.

The minimum values for P can be computed as follows:

$$4.)\ P(\min) = Po * (1 - (Tin + Ttn + Tan + Trn + Ton)/100\%)$$

The maximum values for P can be computed as follows:

$$5.)\ P(\max) = Po * (1 + (Tip + Ttp + Tap + Trp + Top)/100\%)$$

The P(min) tolerance subscripts include an "n" and the P(max) tolerance subscripts include "p" to indicate that the variables may be biased (that is, Tin may not equal Tip in magnitude). For random variables, Ti = Tip = Tin.

b. RSS Constituent Parameters

To calculate the "P" parameter limits (maximum and minimum values of P), the tolerances of each constituent parameter are separated into bias and random variable terms. Each is summed with CPs in the same category:

Categories of "P" Parameter Error Used in the *P(WCmin)* and *P(WCmax)* Equations:

Positive Biases (PB): Units of percent. These are non statistical terms that are not included in the RSS summation. Example: These would include the mean "P" parameter error that increases with temperature. If a "P" parameter error positive change with temperature is specified with a maximum and minimum, the mean would be added to the positive bias terms and the delta error divided by 2 would be included in the RSS error computed at the circuit level.

Negative Biases (NB): Units of percent. These are non statistical terms that are not included in the RSS summation. Example: These would include the mean "P" parameter error that decreases with temperature. If a "P" parameter error negative change with temperature is specified with a maximum and minimum, the mean would be added to the negative bias terms and the delta error divided by 2 would be included in the RSS error computed at the circuit level.

Random Terms (RT): Units of percent. This is the statistical portion of the error that is combined using RSS methods. These terms include delta errors divided by 2 mentioned in the positive and negative bias paragraphs.

Pmin and Pmax are calculated by summing like terms of Ti, Tt, Ta, Tr, and To in the manner shown in equations 6 through 8 and then applying equations 9 and 10 to derive the "P" parameter. Po is the nominal parameter value:

$\sqrt{\sum(Random\ Terms)^2}$ (Units of %):

$$6.)\ T(RT) = \sqrt{\sum (RT)^2} = \sqrt{Ti(RT)^2 + Tt(RT)^2 + Ta(RT)^2 + Tr(RT)^2 + To(RT)^2}$$

$\sum Negative\ Biases$ (Units of %):

$$7.)\ T(NB) = \sum Neg\ Biases = Ti(NB) + Tt(NB) + Ta(NB) + Tr(NB) + To(NB)$$

$\sum Positive\ Biases$ (Units of %):

$$8.)\ T(PB) = \sum Pos\ Bias = Ti(PB) + Tt(PB) + Ta(PB) + Tr(PB) + To(PB)$$

$$9.)\ P(WCmin) = Po * [1 - \sum Negative\ Biases - \sqrt{\sum (Random\ Terms)^2}\ ]$$

$$10.)\ P(WCmax) = Po * [1 + \sum Positive\ Biases + \sqrt{\sum (Random\ Terms)^2}\ ]$$

Short hand versions of equations 9 and 10:

11.) P(WCmin) = Po - P(NB) - P(RT)

12.) P(WCmax) = Po + P(PB) + P(RT)

The P(WCmin) and P(WCmax) parameters used in the circuit level analyses are in terms of parameter (resistance, capacitance, volt ref, etc.). All terms starting in "T" are in units of percent or %/100. The conversion from "T" to "P" terms are shown in equations 9 and 10.

Constituent Parameter (CP) Statistical Considerations

The Ti(RT) terms are that portion of the constituent parameters that have statistical distributions. The distributions considered for each of these CPs are normal (ND), truncated normal (TND), and uniform distributions (UFD). Examples are shown in Figures 6, 7, and 8.

The allowable probability of exceeding the RSS limits for each constituent parameter (CP) is 0.0027 (3 sigma normal probability). The "P" parameter error includes an RSS summation of the CP "T" parameters. The "P" parameter distribution is therefore a composite mixture of these distributions that will roughly take the shape of a normal distribution. The two extremes of this composite "P" parameter distribution are the normal distribution and the multi uniform variable (MUV) distribution. The actual "P" parameter distribution would lie somewhere in between. The Uniform Distribution UFD MUV distribution is visually similar to the normal distribution.

Definitions of PDF, which is shown in Figures 3, 4, and 5.

Density Function (PDF): Derivative of the distribution function with the random variable (RV).

$$PDF = d(\text{Distribution Function})/d(RV)$$

Distribution Function: Integral of the PDF with the random variable RV. Where the $P(RV = -\infty) = 0$ and $P(RV = +\infty) = 1$. The actual probability between $-\infty$ and RV are calculated with the distribution function.

Random Variable (RV) is that portion of the CP that inputs to the RSS part parameter summation.

- Additional information on uniform distributions is in Appendix L Sub-Appendix Section 2.2

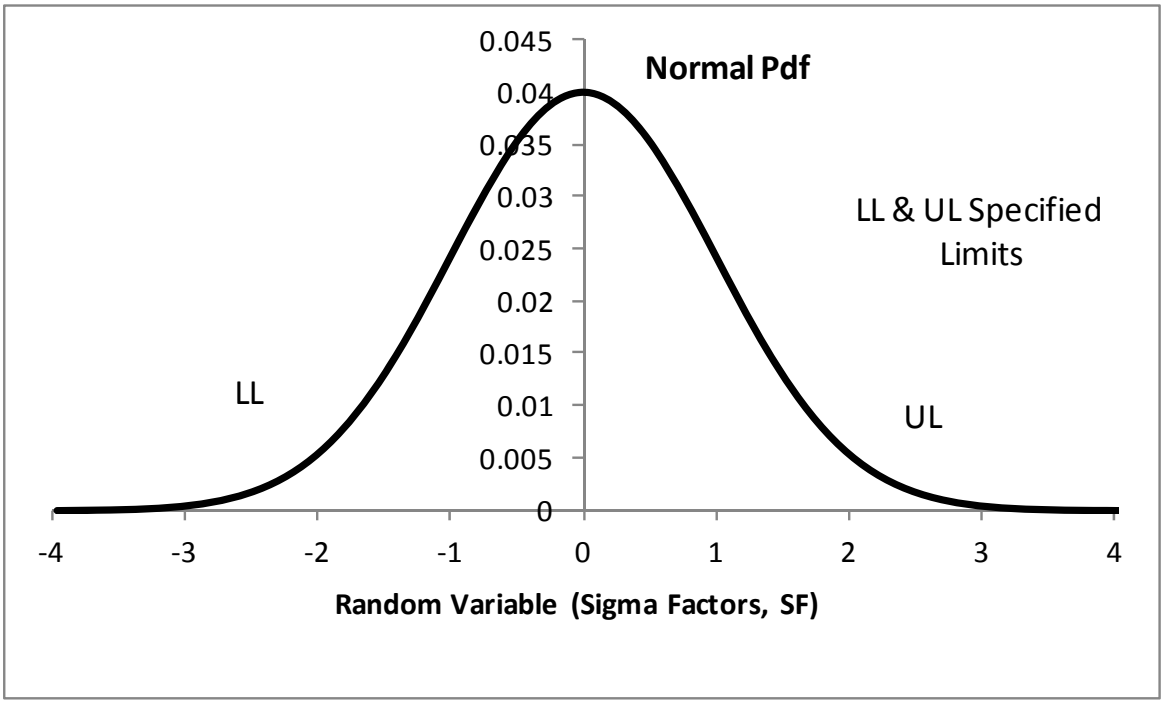

Figure 6. Normal distribution.

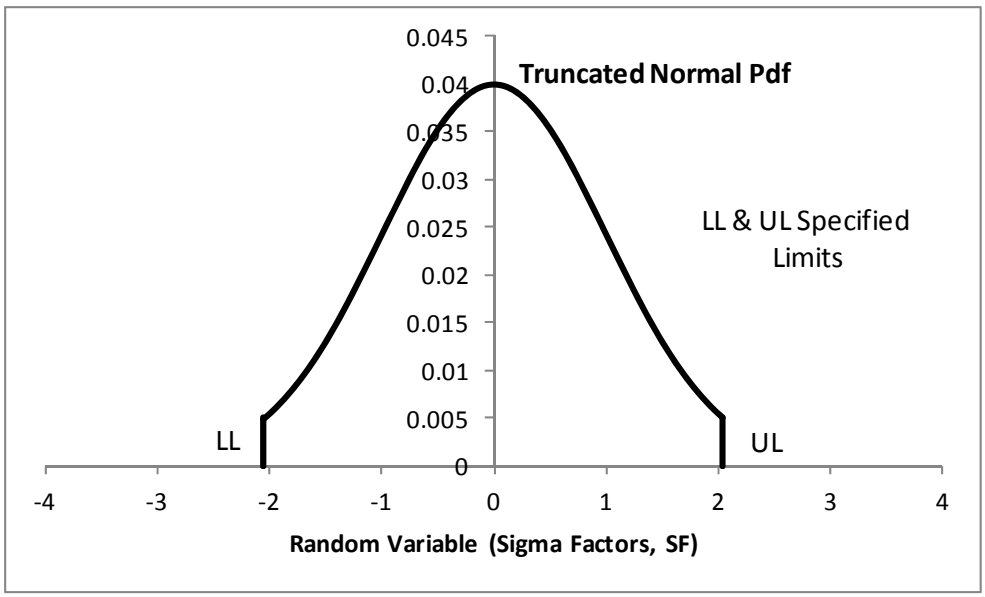

Figure 7. Truncated normal distribution.

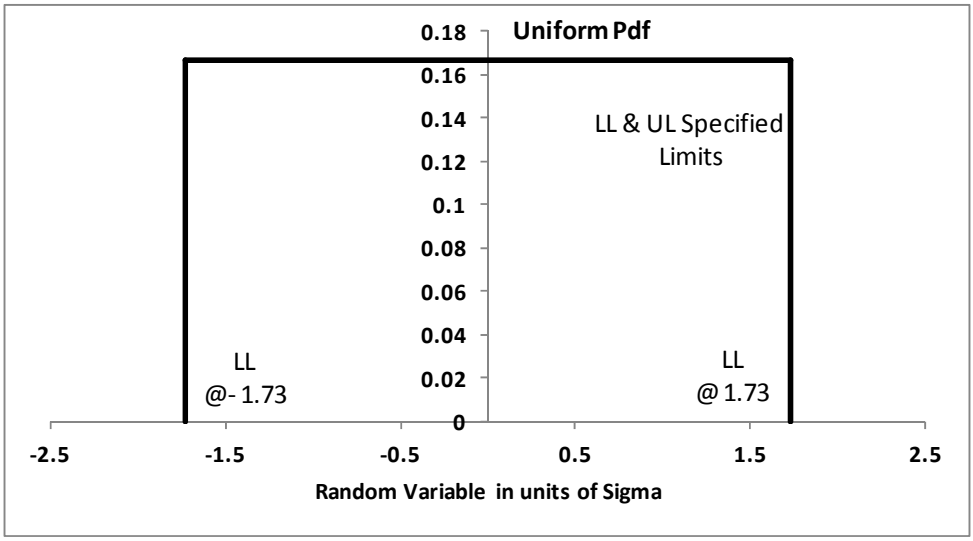

Figure 8. Uniform distribution.

Level 1 (Part parameter derivation) is the only level where the statistical distributions are introduced and the level 2 (Circuit Vo derivation) and level 3 (Multi circuit output derivation) circuit output distributions are a function of these distributions.

Additional information on CP and "P" parameter statistics is found in Appendix L Sub-Appendix A Section 2.1.1. Appendix L Sub-Appendix B Section 2.0 provides an example of deriving "P" parameters by the RSS and EVA summation of CPs.

Circuit Level Component Error Summation

Once the level 1 (part parameter) variations have been calculated, the next step is to derive the circuit-level variations. This is level 2 in the statistical WCCA flow (Figure 3 in section IIIF). The level 2 outputs are the worst case limits of the circuit output, referred to in this section as Vo.

Once the worst-case *{min, max}* range for the "P" parameters have been determined, the next step is to show how to apply the parameters. Equation 13 is the general equation for the circuit output Vo:

$$13.)\ Vo = f(p_1, p_2, \dots, p_n, E_1, E_2, \dots\ , E_m).$$

Note: When performing circuit level calculations, keep track of how biased parameter variations are being calculated. It is common to simply take the worst case value for each part, even though the worst case values occur under different conditions. For example, one part may be at its maximum value at highest temperature while another part may be at its maximum at minimum temperature. These overly conservative calculations generally may make WCCA easier to perform, but if the WCCA results fall outside the allowable limits, revisit the analysis to see if any impossible combinations can be eliminated.

The guideline describes 4 basic level 2 (Circuit level output derivation) summation methods. Only one of these methods is discussed in Section G, which is the statistical large signal analysis. The other analysis types are described in Appendix L.

1. Statistical large signal analysis
2. EVA large signal analysis,
3. EVA Small Signal analysis
4. Statistical Small signal analysis

The small signal analyses are sometimes called sensitivity analyses. There are two parts to the large signal statistical analyses, which can use Monte Carlo (MC) or root sum squared (RSS) methods.

Appendix L Sub-Appendix B Section 3.0 provides an example of each summation type.

Acceptable Probability for Circuit Level Outputs Exceeding WCCA Limits:

The acceptable probability for both the level 2 (part parameter derivation) and level 3 (circuit level output derivation) circuit level outputs exceeding the RSS calculated limits is 3 sigma normal. This means the probability of any one of these outputs exceeding the limits calculated in a RSS analyses is less than 0.0027, which is equal to the probability of exceeding the normal distribution probability of being outside $\pm$ 3 sigma. This standard is the success criteria used for all the following RSS guidelines. Refer to Appendix L Sub-Appendix A Section 2.1.1 for additional details.

Large Signal Analysis Statistical Foundation

There are two large signal analysis methods addressed in the guideline, which are:

1. Large signal RSS analysis performed with the Spice simulator
2. Monte Carlo analysis performed with the Spice Simulator

   The details of the process are addressed in Appendix L Sub-appendix A Table 4: Guideline for the implementing the Spice RSS method provides the detail process. An abbreviated version of the process for computing Vo follows:

   1. Compute Vout with all part parameters (Rs, Ls, Cs, Vref, gains, etc.) nominal. Vout = uo

2. Calculate Vo1+ for all part parameters nominal except parameter 1 (P1) varied to the positive extreme and then calculate Vo1- for the negative extreme.
3. Calculate all other Voi+ and Voi- terms using the same step 2 procedure.
4. For each part parameter and excitation variable calculate the mean and delta (random variable) values:

14.) $Mean = Voim = ([Voi+] + [Vo-])/2$
15.) $Delta = Void = ([Voi+] - [Vo-])/2$

5. Calculate Vout(RSS) with equation 16.

16.) $Vout(RSS)$
$= \sqrt{\{(Vo1d - uoa)^2 + (Vo2d - uoa)^2 + (Vo3d - uoa)^2 + \cdots (Void - uoa)^2\}}$

uoa: The average value of all the Voim terms.

Vout(RSS): Vout(RSS) can be computed with equation 17 using the data derived in steps 1 – 4.

6. The resulting Vo range can be computed as follows:

17.) $uoa - Vout(RSS) < Vout < uoa + Vout(RSS)$

3. Monte Carte Carlo Analysis
The details of the process are addressed in Appendix L Sub-appendix A Table 6, which is the guideline for implementing the Spice Monte Carlo (MC) method. The basic foundation for the MC analysis is presented as follows. Examples of Monte Carlo circuit analysis for different parameter distributions and interval calculation methods are presented in Appendix L Sub-appendix B Section 3.0.

Monte Carlo WCCA Methods and Statistical Foundation

A Monte Carlo (MC) simulation generates a mean (u) and a standard deviation (σ), which are two of three parameters needed to compute the Vo limits. The third parameter is a constant Kp, which is sigma multiplier, that determines the probability of Vo exceeding the Vo limits.

The desired maximum probability of being outside the WCCA computed limits has been set at 0.0027, which is the two tail normal distribution 3 sigma probability. Assuring the probability of exceeding the Vo limit is less than .0027 is determined by the selection of Kp.

The limits of the circuit output parameter, Vo, derived using the MC analysis is expressed in equation 18:

18.) $u - Kp * \sigma < Vout < u + Kp * \sigma$

Monte Carlo (MC) Vo Distribution Assumptions: There are three methods that are used to compute Kp. Two of the methods assume the distribution of the Spice MC output is Gaussian, which is the likely output distribution because the part parameter tolerances are Gaussian. If a non-linearity such as signal squaring function, multiplication of two signals, logarithmic gain or some other signal distortion, is introduced into the simulation, the distribution will not be pure Gaussian. In this situation a third method of computing Kp from the MC data will be required, which is termed the

distribution free method and will be addressed herein. The first method to be addressed is Prediction Intervals (PI).

Prediction Intervals: Prediction interval (PI) statistics are used for determining the limits of circuit operation from a MC data output. Kp calculated using PIs approaches 3.0 as the number of MC data points (n) increase. The process for calculating PIs is shown in below. A plot of Prediction interval Kp's are plotted versus Degrees of Freedom is shown in Figure 9 (DOF = n – 1, where n is the number of Monte Carlo runs). The definition of Prediction Intervals is as follows:

Prediction interval Definition: The range of Vo limits between which there is a 0.9973 (= 1 - 0.0027) probability that Vo will occur. Note, that in general, a PI can be generated for a wide range of desired probabilities and any number of samples.

Prediction Interval Computation Procedure – "tinv" is calculated with Microsoft Excel

1. Derive the Vout mean (u) and standard deviation (σ) directly from the Monte Carlo (MC) PSpice output data.
2. Compute Kp = Sqrt((DOF+2)/(DOF +1))*tinv(P,V) = Sqrt((n+ 1)/(n))*tinv(P,V)
    a. P = .0027 = 1 – (99.73 %/100%), Probability of Vout being outside the PI.
    b. V is the number of degrees of freedom = DOF = n -1, n is the number of MC data points.
    c. tinv is the "t" distribution inverse function

        Numerical values for the tinv function can be derived from Excel. The Excel path is as follows: Open Excel/formulas/more functions/statistical/tinv.
3. Compute the Vout circuit range of operation with the following equation:

$$19.) \quad -Kp * \sigma + u < Vout < Kp * \sigma + u$$

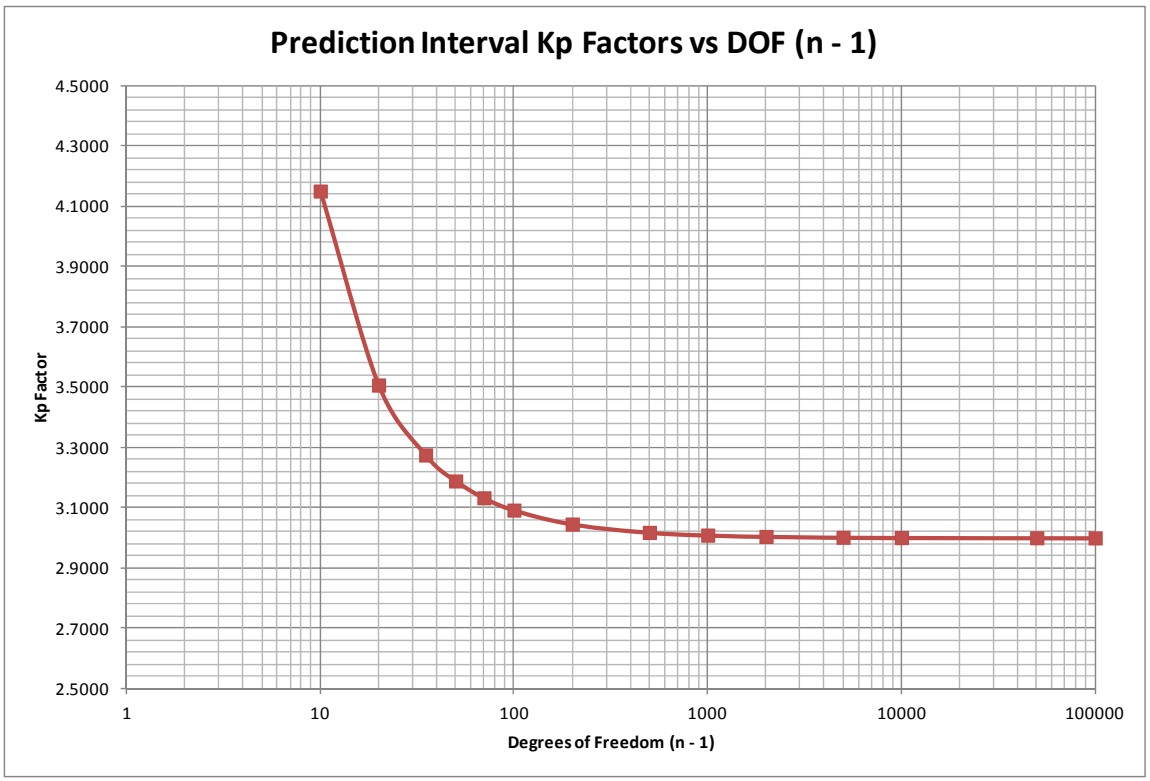

Figure 9. Kp versus Degrees of Freedom(DOF = n – 1) for prediction intervals. For "n" MC runs, the probability of exceeding Vo limits using Kp from this graph is .0027 (3σ 2 tail normal). Kp assumes that the probability distribution derived from the MC data is Gaussian.

Tolerance Intervals – An alternate method of calculating the K factor is with tolerance intervals (TI), which is referred to as Kt.

Tolerance Interval (TI) Definition: The range of values within which there is a 90 % (= Confidence limit (CL)) confidence that 99.73 % (P*100%) of the past and future Vo's will reside. Note, that in general, a TI can be generated for a wide range of Confidence Limits (CL), a wide range of P and any number of samples. P and CL can be modified to suit individual program requirements. Reference 3 at the end of this Section G shows the how TIs can be applied to other requirements.

Prediction intervals are favored over tolerance intervals for the following reasons.

1. TIs yield an overly conservative wider RSS range and could unnecessarily cause a design modification or unnecessary part upgrade.
2. TIs require 10X more MC runs to converge within 3% of 3 sigma normal.
3. The TI is defined as the range for which there is some probability (90%) that some percentage of future unit Vo measurements (99.73%) will fall. 90% is an arbitrary number, which is far too low, but if increased will widen the interval even more.
4. What is needed is an interval (PI) for which there is some probability (99.73%) that a single Vo will reside.
5. PIs are consistent with probability of failure computed in a reliability analysis, in that if Vo exceeds its RSS limits, the probability of failure increases above the allowable .0027. The

probability of Vo staying within the PI limit and not failing is consistent with hardware reliability.

Note: If for some reason, TIs must be used in a present application, phasing out TIs in favor PIs in all future applications is recommended.

The Vo limits are computed with equation 20 which is identical to equation 19, except the subscripts are changed from "p" to "t".

20.) $-Kt * \sigma + u < Vout < Kt * \sigma + u$

The Sigma (σ) and the mean (u) are derived directly from the MC data output. Kt is derived by the guideline shown below.

Additional information on Tolerance Intervals is discussed in Reference 3 at the end of this Section G.

Figure 10 shows a plot of Kt versus degrees of freedom (n – 1), where n is the number of Monte Carlo runs using prediction intervals. Figure 4 aids in selecting the number of runs for the Monte Carlo analysis.

As the number of MC runs increase, Kt approaches 3.0. (3.0 corresponds to the normal distribution 2 tail 3σ points) A plot of Kt versus the number of MC runs is shown in Figure 4.

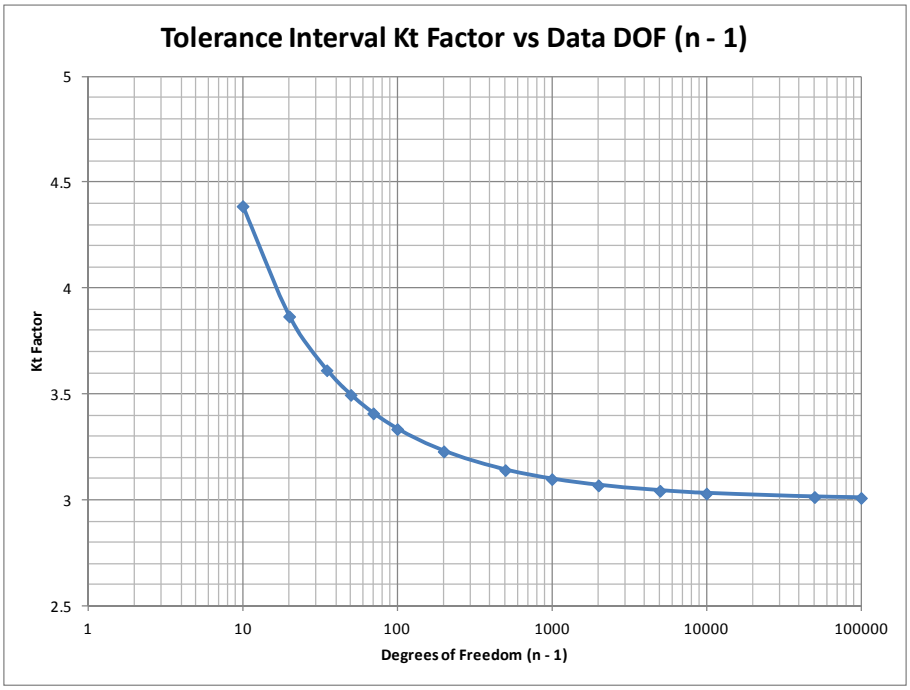

Figure 10. Kt Factor Versus Degrees of Freedom (n – 1), where n is the Number of MC Runs. For "n" MC runs, there is a 90% confidence that 99.73 % of the Vo's will fall inside the tolerance interval. Kt assumes that the MC probability distribution derived from the MC data is Gaussian.

Tolerance Interval Computation Procedure (Website)

1. Compute the upper (UL) and lower (LL) WCCA limits (Kt*σ) using the following Website: http://statpages.org/tolintvl.html
2. Derive the Vout mean (u), standard deviation (σ) and number of runs (n) directly from MC PSpice output data.
3. Input the following into the website work sheet 5 cells:

   Number of samples

   Mean

   Standard Deviation

   % Certain (90%)

   % Population (99.73%)

4. The output is taken from the cell labeled: "a two sided Tolerance Interval"
5. Equation 14 shows the Vout Monte Carlo Tolerance Interval range with the website derived upper and lower limits:

   14.) $LL < Vout < UL$

Definitions:

$$LL = -Kt * \sigma + u$$

$$UL = +Kt * \sigma + u$$

Equivalent expressions for equation 14 Vo(WC) are shown in equations 21 and 22, which can be applied to the Level 3 Multiple Circuit Analysis:

21.) $Vo(WCmin) = Vnom - Kt * \sigma$

22.) $Vo(WCmax) = Vnom + Kt * \sigma$

Definitions:

Vnom: Mean (u) derived from the MC Runs.

σ : Standard deviation derived from the Monte Carlo runs.

Kt: Factor derived from the number of MC runs (n) and allowable probability of exceeding the Vo(WC) range using prediction interval statistics.

Below is an alternate method for computing Kt as backup to using the Table 4 Website based procedure, in the event the Website is not available in the future. The alternate method of computing Kt using Matlab provides more insight into the statistical basis for tolerance intervals. The probability distribution used in the Matlab method is the non central "t" distribution.

Alternate Tolerance Interval Computation Procedure (Matlab)

1. Derive the Vout mean (u) and standard deviation (σ) directly from MC PSpice output data.
2. Compute Kt with equation 23.

   23.) $Kt = nctinv(P, NU, Delta)/Sqrt(DOF - 1)$

   Definitions:

   a. P = Confidence Level (CL) =.9
   b. NU is the number of degrees of freedom = DOF = n -1
      - n is the number of MC data points
   c. Delta = Norminv(X, 0,1)*Sqrt(DOF - 1), X = 1 – (1 - .9973)/2 = .5 +.9973/2
   d. Numerical values for the norminv function can be derived from Matlab. The "norminv" function is also available on Excel. The Matlab path is as follows: Open Matlab, double click on fx, scroll down to statistical tool box/probability distributions/Inverse cumulative distribution/norminv. 99.73 % is the estimated percentage of past and future events residing within the tolerance interval.
   e. nctinv(P,NU,Delta), "nctinv" is the non central "t" inverse function.
   f. Numerical values for the "nctinv" function can be derived from Matlab. The "nctinv" function is not available on Excel. The Matlab path is as follows: Open Matlab, double click on fx, scroll down to statistical tool box/probability distributions/Inverse cumulative distribution/nctinv
3. Compute the Vout circuit limits of operation equation 24:

   24.) $-Kt * \sigma t + ut < Vout < Kt * \sigma t + ut$

   A convenient tool for determining the number of runs required to give a particular confidence interval and confidence level using the Tolerance Interval method can be found at http://statpages.org/tolintvl.html.

Distribution Free Intervals – PIs and TIs assume the Spice MC output is Gaussian. If the Spice MC output is not Gaussian the distribution free interval (DFI) method may be applied. A complete description of DFIs is presented in Appendix L Sub-appendix A. DFIs are needed when the MC output is not Gaussian and can take any number of forms, which are as follows:

1.) Flat distributions, which approach the uniform distribution in the extreme case.

2.) Skewed distributions due to such causes as the output signal being squared or processed with log function or exponential functions.

3.) Distorted signals caused by amplifier saturation.

In these cases, a probability distribution is derived directly from the Monte Carlo n data points. No standard deviation or mean average values are required to derive the DF interval. Table 3 list steps required to compute the DF probability of exceeding the calculated limits.

Table 3 – Distribution Free Limit Calculation

1. Display the Vo data points below the Spice Monte Carlo histogram output.
2. Steps for calculating the probability from the MC data output results.
    a. Copy the Vo data from step 1 into Microsoft Excel.
    b. Order the Vo numbers from low to high
    c. Assign a rank to each Vo number. The lowest number will have a rank of 1 and the highest will have a rank of n, where n is the number of Vo data points transferred.
    d. Divide each rank number by n, so the ranking numbers range from 1/n to 1. This is the fractional ranking.
    e. Plot the fractional ranking vertically (Probability) and the Vo data horizontally (RV).
    f. This is a plot of the $P(-\infty < Vo < RV)$. Probability of I(RMm) being less than RV. Note in this example the Vo parameter is "-I(RMm)".
3. If the distribution properties are not known, several Vo MC data points will be required outside the DF interval limits, which are IH and IL. At least 3 points should be higher than IH and 3 points should be lower than IL. The number of MC runs required to meet this criteria is as follows: n > 3 points/(.0027*.5) = 2223 runs.
4. The probability is computed by selecting Vo for P = .00135 and P = (1 - .9973)/2. .00135 is the allowable probability of exceeding the IH limit. .00135 is also the allowable probability of being outside the IL limit.

The following is a 1000 data point example using available Gaussian data, which illustrates the process. Instead of 3 data points outside IL & IH, there is only 1. Figure 11 shows a plot of a typical Monte Carlo histogram of the random variable "-I(RMm))" and the circuit modeled. I(RMm) is the output current through the lower right hand resistor. The MC Spice output file includes the 1000 "-I(RMm)" data points right below the histogram. Figure 12 shows the Excel plot of the probability distribution curve, derived from the Spice Monte Carlo data file.

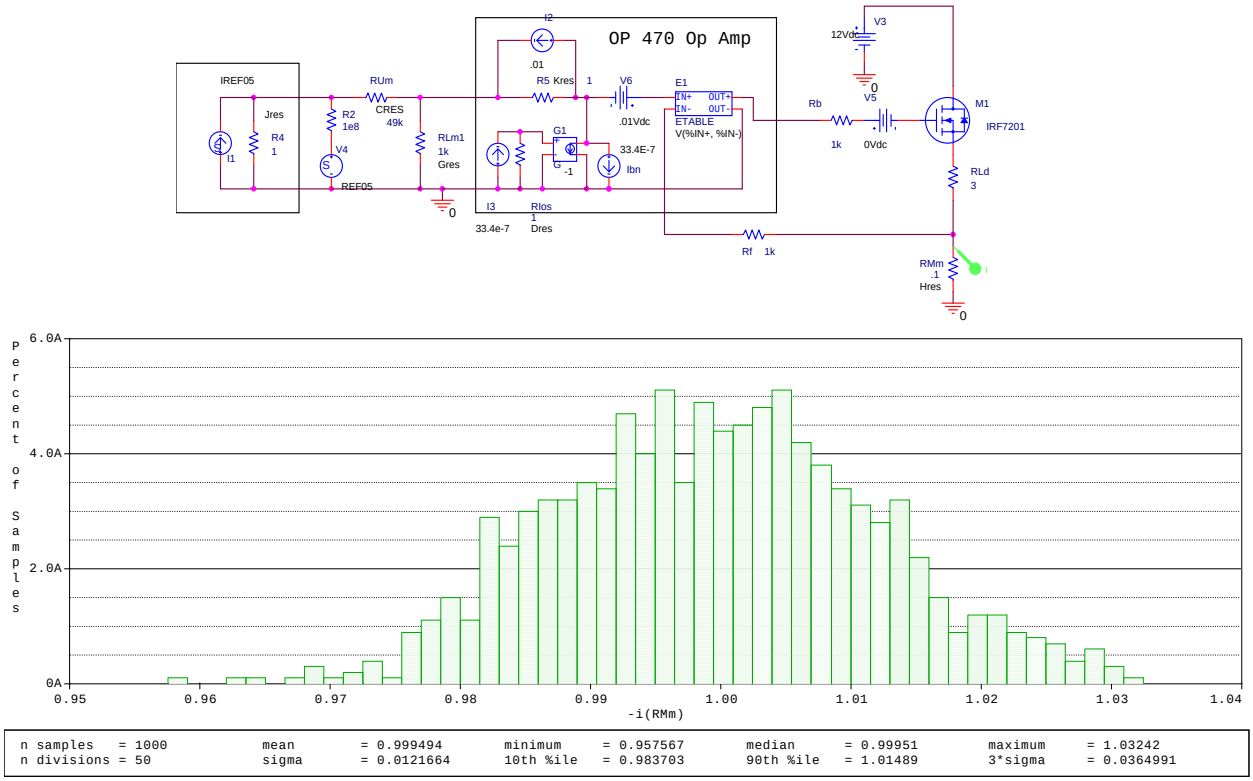

Figure 11. MC histogram showing the –I(RMm) distribution and the circuit analyzed.

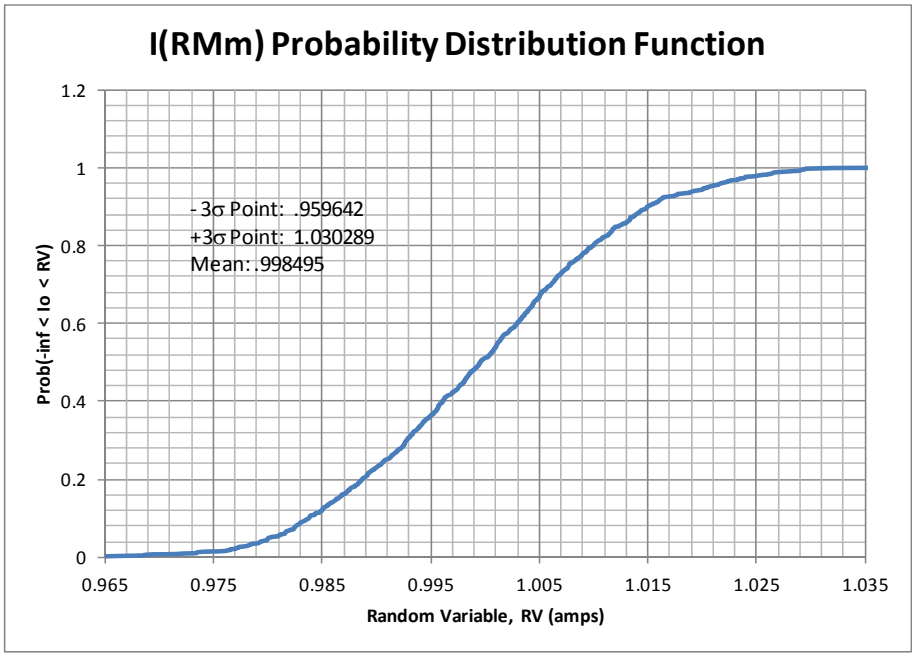

Figure 12. Plot of "–I(RMm)": Probability of "–I(RMm)" being Less than RV.

The limits are derived from the DFI process are as follows:

$$.9596 < -I(RMm) < 1.0303 \; and \; the \; Mean = .9985$$

The number of MC runs in this case is very large (1000) and as a result, there is no need to apply the prediction intervals or tolerance intervals, because the PIs, TIs and ND all converge to the same value for large values of "n".

Risk Reduction Guideline Using Sigma Factors (SF)

Selecting an SF of greater than 1.0 will decrease the probability of Vo exceeding the Vo WC range and also widen the Vo WC range. The desired probability of exceeding the Vo WC limit is less than .0027 (Normal 3 sigma probability). If the risk of Vo exceeding the Vo WC range is considered too high, then applying an SF greater than 1.0 should be considered. Figure 13 plots an estimated probability factor improvement for SFs between 1.0 and 1.73 to give some idea of the SF impact. Note if SF = 1.1, the factor decrease in probability is 2.4. The probability of Vo exceeding the Vo WC limits would decrease from .00648 to .0027. If SF = 1.2, the factor improvement is 4.8 and the probability decrease is .01296 to .0027.

The following should also be considered in the selection of SF:

1. Consequence of exceeding Vo WC limits.
2. Assess past experience with Vo exceeding correctly calculated RSS limits. The assessment includes reviewing past circuit applications and determine if any output parameters ever exceeded the Vo limits computed with RSS.
3. Knowledge on how the part manufacturer performs 100% screening of some parameters, sample tests of other part parameters, lot qualification testing and the associated fallout will reduce the uncertainty on the sigma location of the CP parameter limits.
4. Customer preference on the allowable risk of exceeding limits.
5. Method of computation of the "P" parameters. There is less risk if "P" parameters are computed by an EVA sum of CPs rather than summing CPs by RSS. In the former (EVA) case, there would be very little gained in applying an SF greater than 1.0.

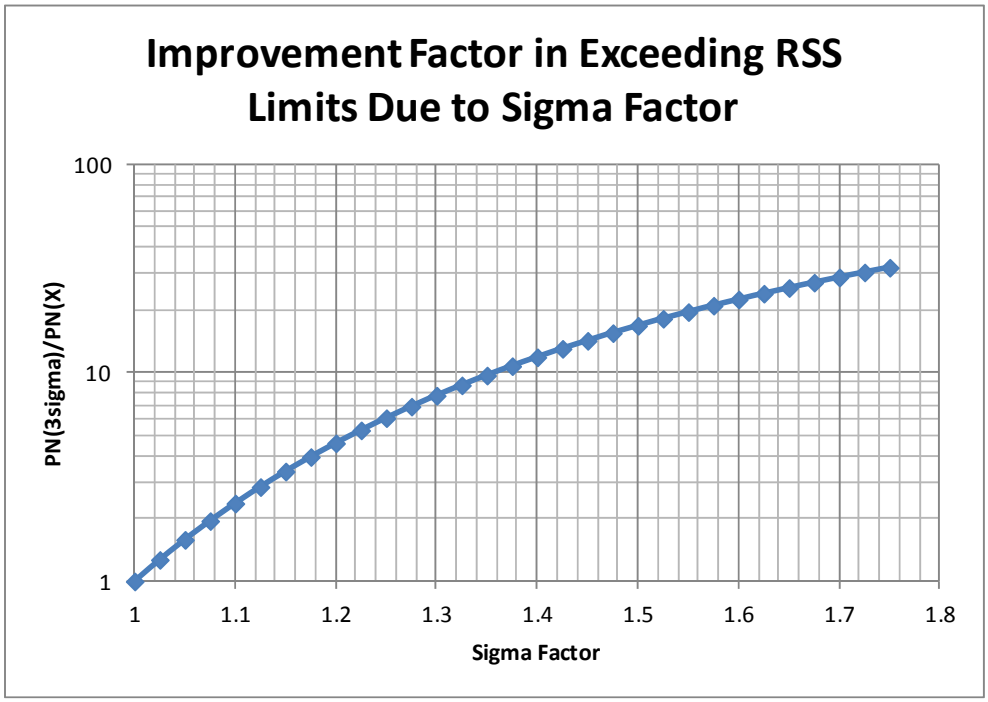

Figure 13. Sigma factor probability improvement factor.

The sigma factors (SF) are applied by multiplying RSS summed errors by the sigma factor for the Monte Carlo and the large signal RSS methods.

The large signal Monte Carlo SF equation 25 derived with Prediction Intervals is the same as equation 19 with the SF applied:

$$25.)\ -SF*Kp*\sigma+u<Vo<SF*Kp*\sigma+u$$

The large signal Monte Carlo SF equations 26 derived with Tolerance Intervals is the same as equation 20 with the SF applied:

$$26.)\ -SF*Kt*\sigma+u<Vout<SF*Kt*\sigma+u$$

The large signal RSS method equations are identical to equation 17, which is derived for the large signal RSS method. Appendix L Sub-Appendix A also addresses large signal RSS multiplied by SF in more detail.

$$27.)\ uoa-SF*Vout(RSS)<Vout<uoa+SF*Vout(RSS)$$

Circuit Level Guidelines

1. Number of Random Variables Allowed to be RSS'd: The sum of two or more random variables can be summed using the root sum squared method. Appendix L Sub-Appendix A Section 3.9 explains how the probability of exceeding a two variable RSS is less than or equal to exceeding a 3 variable RSS. In past guidelines, RSSing was limited to 3 variables or more and as a result, a mathematical derivation is provided to show RSSing 2 variables is acceptable. One concern when only two RVs are RSS summed is that extreme values could line up and cause an EVA WC summation, which is true. However the odds of two parameters (X1 & X2) being in the WC range simultaneously is less than 1.8E-6 (= .00135*.00135). The WC range is anything greater than +3σ and anything less than -3σ. Probability of X1 between 3 sigma or higher is .00135. (single tail 3σ normal probability). The same is true for X2. As a result, the probability of X1 and X2 adversely lining up is sufficiently low (1.8E-6) to allow two variables to be RSS'd.

    a. Correlated Parameters

    In the foregoing and following guidelines involving statistics, the "P" parameter and CP random variables are assumed to be totally independent and zero correlation is assumed between any two variables. In most cases, if there is correlation between two parameters, the RSS range computed without correlation will be worse or wider than the range with correlation. For the most part, correlation between parameters need not be considered unless RSS without correlation does not result in acceptable margin. Although the net effect of correlation on the RSS and the bias terms will likely increase margin, increased margin cannot be guaranteed and the possibility of adverse effects on margin cannot be dismissed. Margin is defined as the difference between the RSS limits and the allowable limit.

    An example of parameter correlation is as follows: Timing analyses involving logic integrated circuit (IC) propagation delays, rise times and fall times are very likely not independent. These timing parameters will track with power supply voltage and temperature. Timing parameters will also track part to part. As an example: all prop delays in logic IC A will tend to be larger than the prop delays in logic IC B. (Logic ICs A and B have the same part number.) In general, considering correlation between propagation delays will increase timing margins compared to not considering correlation.

To consider part to part correlation between parameters, sufficient test data must be acquired enabling 1) the derivation of equations of one parameter as a function of a correlated parameter and 2) the calculation of the resulting residual statistical error. The data must be acquired for each manufacturer's lot date code and parts from the same lot date code must be installed in a given piece of hardware. As a result, correlation is only practical for a very small number circuit builds, where part manufacturer and LDC control can be assured during the installation process. RSS with parameter correlation should be considered third in the order of computational preference. The order is:

1.) EVA

2.) RSS without correlation

3.) RSS with correlation

Correlation between parameters is a candidate subject of future guideline updates with a recommended focus on the following: exceptions to correlation narrowing RSS limits, modeling correlation between part parameters and how to apply the correlated parameters to Spice models.

b. Other Types of Electronic Analyses

There are other types of analysis that can be performed on analog and power circuits other than steady state DC. Statistical and RSS analysis can be applied AC and transient analyses. Various parameters can be assessed such as amplifier bandwidth, amplifier gain, amplifier phase response, phase and gain stability margins and others.

c. Other Types of Electronic Circuits

There are other types of circuits that can be analyzed using the foregoing techniques other than steady state DC analog circuits. Logic timing analysis can be performed using RSS manual methods only. At this time, there are no reports of logic simulators that can perform Monte Carlo timing analysis. Monte Carlo logic timing analysis is a subject of future guideline updates with a recommended focus on utilizing the existing PSpice Monte Carlo capability.

d. Multi - Modal Distributions

Multi - modal CP parameter distributions are possible anytime different part manufacturers are mixed or lot date codes are mixed. Each CP with a multi - modal distribution can be bounded by a single normal distribution with specified limits set at the 3 sigma limit assuming the following:

1. Each of the single distributions (SD) making up the multi-modal distribution are normally distributed with specified limits set at 3 sigma or greater.

2. All the SDs can be assumed to have similar distributions, because no matter what lot date code or manufacturer, the fabrication process and materials are similar.

Additional supporting information is in Appendix L Sub-Appendix A, paragraph 3.9.

In addition to these subjects, Appendix L Sub-appendix A addresses the following issues: Large variation parameters, Statistical distributions other than ND, TND and UFD.

4. Multiple Circuit Error Summation

   There are three levels of WCCA Integration listed in Figure 3 of Section IIIF and level 1 (derivation of part parameters) and level 2 (Derivation of circuit output parameters) have been addressed in detail. The level 3 (Multiple circuit output derivation) guidelines show the allowable methods for integrating the level 2 (circuit level Vo derivation) output to derive the level 3 multiple circuit output, Vm.

   A multiple circuit example is three voltage reference circuits (Vo1, Vo2 and Vo3, which are not necessarily identical) connected in series and the objective is to find the limits of Vm, which is the sum of the three voltages using EVA and RSS methods. Assuming that each circuit can be considered standalone and there is no concern with interactions between circuits due to loading or other effects, then Vm is the sum of the three nominal voltages shown in equation 29.

   $$29.)\ Vm = Vo1 + Vo2 + Vo3$$

   The EVA extremes of the total output would be the sums of the positive and negative deltas added to the nominal total voltage. The deltas could also be RSS summed with the nominal voltage to give the RSS overall Vm range. The level 2 circuit parameters (Vo1, Vo2, and Vo3) may be algebraically added as shown in equation 29 or RSS'd as shown in equation 30.

   $$30.)\ Vm = Vm(nominal) + \sqrt{Vo1^2 + Vo2^2 + Vo3^2}$$

   Vm(Nominal = Vo1(Nominal) + Vo2(Nominal) + Vo3(Nominal)

   Any combination of RSS and addition are valid mathematically. Below is a summary of the allowable methods for combining multiple circuit outputs. Any of these methods of summation are acceptable. The statistics associated with Table 7 can be summarized as follows: The Vo1 sigma is greater than the lowest sigma of the individual circuit outputs (V(RSS1), V(RSS2) and V(RSS3)) or the Vo1 probability of exceeding RSS limits is less than the probability of any of the individual outputs of exceeding its RSS limits. Refer to Appendix L Sub-Appendix A Section 4.0 for additional details on statistics and on the relationship between individual outputs and multiple circuit outputs. Note that V(RSS1) is the RSS portion of Vo1 as shown in equation 31.

   $$31.)\ Vo1 = Vo1(mean) + V(RSS1)$$

   Vo1(mean): Mean value of Vo1

   V(RSS1): Random variable of Vo1

   So if the probability of Vo1 exceeding V(RSS1) is 3 sigma, then the probability of Vo1 exceeding Vo1(RSS) is less than the 3 sigma probability.

Allowable Options for Integrating Multiple Circuit Outputs

1. RSS1 – RSS2 – RSS3: Vo1 = SQRT[$V(RSS1)^2$ + $V(RSS2)^2$ + $V(RSS3)^2$]
   If RSS1 has the lowest sigma (most probable to exceed RSS limit) of RSS1, RSS2, and RSS3, then sigma(Vo1) > sigma(V(RSS1)) and therefore Vo1 is less likely to exceed RSS limits compared to V(RSS1).

2. RSS1 – RSS2 – Add3: Vo2 = SQRT[V(RSS1)^2 + V(RSS2)^2] +V(ADD3)
   If RSS1 has the lowest sigma of the RSS1 and RSS2, then sigma(Vo2) > sigma(V(RSS1)) and therefore Vo2 is less likely to exceed RSS limits compared to V(RSS1).

3. RSS1 – Add2 – Add3: Vo3 = V(RSS1) +V(ADD2) +V(ADD3)
   Sigma(Vo3) > Sigma(V(RSS)) and therefore Vo3 is less likely to exceed RSS limits compared to V(RSS1).

4. Add1 – Add2 – Add3: Vo4 = V(ADD1) +V(ADD2) +V(ADD3)
   This is the pure EVA case, with the lowest probability of exceeding the WCCA limits.

5. Summary

   The following addresses RSS and EVA options that have been left to the end to benefit from the understanding gained in the foregoing discussion of the WCCA statistical related subjects.

   Table 4 shows eight options for RSS/EVA calculations and all eight options are valid from a statistical and mathematical standpoint. The table addresses all three Section IIIF Figure 3 levels and the approximate probability of the output parameter from each level exceeding its calculated WCCA limits. The most conservative lowest risk option is at the top and the least conservative is at the bottom of the table. The probability estimates are based on the probability of Vout exceeding limits being no greater than the probability of the worst case CP exceeding its limits. The statistical backup and additional details are found in Appendix L Sub-Appendix A Section 4.0.

Table 4. RSS/EVA Options

Option Number	RSS/EVA Options	Level 1	Level 1 Prob of (-RSS >P > RSS)	Level 2	Level 2 Prob of (-RSS > Vo > RSS)	Level 3	Level 3 Prob of (-RSS > Vm > RSS)
1	All EVA	EVA	~0	EVA	~0 %	EVA	~0
2	1 RSS/2EVA	RSS	~ .27% (~ 3σ)	EVA	< .27% (> 3σ)	EVA	< .27% (< 3σ)
3		EVA	~0	RSS	~ .27% (~ 3σ)	EVA	< .27% (< 3σ)
4		EVA	~0	EVA	~0	RSS	~ .27% (< 3σ)
5	2 RSS/1EVA	EVA	~0	RSS	~ .27% (~ 3σ)	RSS	~ .27% (~ 3σ)
6		RSS	~ .27% (~ 3σ)	EVA	< .27% (< 3σ)	RSS	< .27% (< 3σ)
7		RSS	~ .27% (~ 3σ)	RSS	~ .27% (< 3σ)	EVA	< .27% (< 3σ)
8	All RSS	RSS	~ .27% (~ 3σ)	RSS	~ .27% (~ 3σ)	RSS	~ .27% (~ 3σ)

Option 1 uses the EVA summation only and is the simplest approach and should be performed first. If the option 1 WCCA Vout calculated limits do not meet the allowable range of outputs, there are 7 other options. The most reasonable and recommended is option 5, which applies EVA methods to the Level 1 constituent parameters and RSS to Level 2 (Resistors, capacitors, Vrefs, etc) and Level 3 (Individual circuit outputs).

Option 5 recommends EVA summation of CP parameters at level 1 (part parameter derivation) and is the best option, because the level 1 output depends on loosely defined constituent parameter statistical distributions. By adding the specified CP limits directly instead of RSSing, inadvertent exceedance of the Level 2 and level 3 RSS limits due to CP distribution uncertainty is all but eliminated.

Option 8 is also viable and can be used if the limits computed using option 5 do not meet circuit requirements. In option 8, levels 1, 2, and 3 each sum variables with RSS methods and have a highest risk of a parameter exceeding RSS limits. As a result, analytical methods, models, and parameters used in the analysis should be independently reviewed to minimize the chances of analysis errors. To the extent possible, data supporting CP tolerance limits should be reviewed. Bread board verification of the circuit model should also be performed. Following the review and verification, if an unsatisfactory risk still exists, a Sigma Factor can be applied as described earlier in Section IIIG and Appendix L Sub-Appendix A.

References:

1. Applied Statistics and Probability for Engineers, Douglas C Montgomery & George C Runger, page 458. Definition of Prediction Intervals.

2. Basic Statistics, Mark J Kiemele et al, page 7-22. Definition of Prediction Intervals.

   Definition of Prediction Intervals (PI): PIs are confidence intervals about the next future event based on an existing set of data.

3. Engineering Statistics Handbook", section 7.2.6.3 Tolerance Intervals for a Normal Distribution, Paragraph entitled," Tolerance factor based on the non central "t" distribution.

4. Statistical Models in Engineering, Hahn & Shapiro, page 101.

H. Documentation

Section VIII of the Draft Standard (Appendix A) contains detailed requirements for the WCCA Data Package deliverable. In addition to comprehensive reports, associated data files of parts data sources, computer simulation files, test data, and so forth, need to accompany the WCCA reports themselves, to allow reviewers access to all the information they will need to perform a comprehensive review.

Section IX of the Draft Standards contains criteria for reviewability of the WCCA deliverables:

1. No prior knowledge of or exposure to the unit under analysis shall be required of the reviewers.
2. The WCCA data package shall be self-contained, requiring no additional outside information for a thorough review.
3. The WCCA data package shall allow for assessment of all equations, procedures, logical steps, etc., by the reviewer, such that the reviewer does not have to independently derive or re-create any of these to be sure of their correctness.

Following the documentation requirements of the Draft Standard, and applying the criteria for reviewability, will result in a vast improvement over the WCCA deliverables of the past, while providing a uniform set of expectations for the industry.

Appendix A.

Draft Standard for WCCA

Foreword

It is known by the community that insufficient design margin due to inadequate Worst Case Circuit Analysis (WCCA) has been implicated in many test failures and orbital anomalies, and that is the reason for the formation of this team under the auspices of the Mission Assurance Improvement Workshop (MAIW), an industry consortium. Inadequate WCCA can arise from many causes, among which are the following:

- inadequate or unsystematic requirements flowdown and tracking
- incomplete decomposition of designs into analyzable units
- incorrect selection of significant parameters or of their End of Life design limits
- omission of key analyses that prove circuit functionality in the absence of formal or explicit requirements
- insufficiently rigorous analysis due to budget, program, and designer biases (intentionally and unintentionally)
- inadequate, difficult-to-review documentation

To help remedy this situation, we present a draft standard encompassing the best practices of WCCA that address the problems noted above. It is hoped by our team that our work would form the basis of a future compliance standard. The language herein may be tailored for purposes of inclusion into Statements of Work (SOW) or Data Item Descriptions (DIDs).

The focus of our work is for Class A space systems; however, we also include in Appendix 3 a guide to tailoring for Classes B, C, and D.

Appendix A
Table of Contents

A.1 Introduction

The process framework presented in this draft standard represents a paradigm shift from the historical approach to WCCA as practiced by most companies. The goal is to make WCCA an integral part of the design process, well-planned and begun early, rather than a task that is done on the tail end of the design process. Traditionally, WCCA has been a deliverable product due at Critical Design Review (CDR), at which time it is already beginning to be more time-consuming and costly to make design changes, should issues surface during the review of the WCCA. Under the new paradigm, a formal WCCA Plan is due at Preliminary Design Review (PDR). This plan provides a road map to the WCCA process; it is coordinated with and approved by the customer, and it provides a clear medium for establishing the rigorous expectations necessary for a sound and thorough WCCA end product. This paradigm has already been applied on one program and has been uniformly lauded as instrumental in clarifying expectations for WCCA between the prime contractor and its subcontractors and vendors.

The basic ground rules for performing WCCA are presented herein, including determination of worst-case conditions and ensuring a statistically-valid analysis approach.

This draft standard also provides clear methodologies to: 1) ensure requirements flowdown and tracking of derived requirements during the WCCA process, 2) maintain a parts database, and 3) produce high-quality, readily reviewable documentation of WCCAs. Well-documented worst-case analyses have value well beyond the initial proof of design – they also serve as a clear design record that will be invaluable for reference, troubleshooting, and training purposes throughout the life of the program.

The focus of this draft standard is unit-level WCCA, but it is also applicable to both lower levels (such as modules or hybrids) and higher levels (system analyses, such as bus stability), as well as for system interfaces.

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A.2 Basic Requirements

A. A Worst-Case Circuit Analysis, consisting of performance analysis and part stress analysis, shall be performed per the requirements of this standard.

B. A WCCA Plan shall be provided, due as a Preliminary Design Review deliverable (typically SDRL), and updated between PDR and CDR as the design nears finalization, per program requirements.

C. The requirements of the program contract shall take precedence over the requirements of this standard.

D. WCCA shall be performed for all new designs.

E. WCCA shall be reviewed for possible impacts and updated as necessary whenever any of the following are true.

   1. When requirements that were previously verified through WCCA become more demanding.

   2. When any circuit is redesigned or modified in such a way as to invalidate elements of the previous WCCA.

   3. Whenever parts are substituted, whether for obsolescence or any other reason, and the new part parameter variations are materially greater than those used in the previous WCCA.

   4. When the previous WCCA used lot-dependent performance data, and different lots are used for the new build that exhibit materially wider parameter variations (either based on the PMP standard or on lot-testing).

   5. When part screening, inspection, or observed failure rates indicate a substantial change in characteristic performance or when a part is procured from a different vendor with different performance characteristics or limits.

Exceptions: 1) circuits deemed to be non-critical, 2) where large margin exists and it is readily apparent that the change will not jeopardize that margin.

F. For heritage designs that are reused, the previous WCCA shall be evaluated to determine the continued validity of each analysis and to ensure that all required analyses are included in the heritage WCCA.

G. When an earlier WCCA was done using assumptions based on test methods that have been superseded or augmented by more perceptive methods, the WCCA shall be redone (for example, until low dose-rate effects on bipolar technology were discovered, WCCA did not consider them. Today we require ELDRS test results to be factored into WCCA).

H. When equipment designed for a lower class of mission is planned to be used in a higher class (e.g., using a Class C design on a Class A or B mission).

I. Some of the requirements of this standard may be satisfied by the contractor's existing design and verification procedures, subject to customer approval.

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A.3 WCCA Plan

The WCCA Plan for an electronic unit or subsystem shall contain the following information:

A. List of applicable documents, such as PMP Standard, SOW, other standards, etc.

B. Design Description

Block diagram(s), hardware descriptions, and a list of design elements (including part and dash numbers, when available) shall be provided. The list includes all physical elements covered by the WCA, such as modules, circuit cards, subassemblies, cables, etc.

C. Detailed List of Circuits and Analyses To Be Performed

1. For each design element, a list of all the circuits contained therein shall be provided, preferably using unique names or identifiers as needed to avoid confusion between similar circuits.
2. For each circuit, a list of analysis types expected shall be provided.
3. Dependent and high-risk or critical analyses shall be identified. Dependent analyses are those whose result is used by other analyses.

The list of analyses should be as complete as practicable for the level of maturity of the design. It is likely that additional necessary analyses may be identified as the WCCA process proceeds; therefore, the list provided in this section is not to be regarded as necessarily complete. New items added during the WCCA process shall be tracked via the WCM. The list of analyses should be largely complete by Interim Review #2 (see section XI.C).

D. WCCA Compliance Matrix (WCM)

1. The WCCA Plan shall contain a WCM of relevant system-level, unit-level, module level, and interface requirements, showing what the applicable hardware is, and how the requirements are mapped to analyses as required to show compliance. The WCM may be a master spreadsheet or database, maintained as part of the WCCA process by a responsible party designated by the Program Manager.

   It is understood that at PDR the design may not be fully mature and thus subject to change; hence, the WCM included in the WCCA Plan is a best effort.

2. The WCM may be organized by physical or functional elements, or in the requirements sequence.
4. When new requirements are formulated during the course of the WCCA process, including local requirements, they shall be added to the WCM.
5. Local requirements generated as part of the WCCA process do not need to be tracked as formal requirements outside of the WCCA process.
6. The WCM shall be maintained and updated during the WCCA process and delivered with the WCCA final reports at CDR, thus providing a summary of analysis results, and the cross-reference between requirements and analyses.
7. The WCM may be an extension of or combined with other requirement/compliance matrices associated with the unit or subsystem under analysis.

E. Multiple Instances

When identical or very similar circuits occur multiple times in a design, a rationale and list of included circuits shall be provided in the WCCA plan when it is believed that a single analysis will suffice, rather than performing separate analysis for each instance. Also, a rationale shall be provided as to how it will be determined which circuit represents the worst case, in the case where circuit loading or environments are different for different instances.

F. WCCA Approach

1. Analysis Methods and Tools

For each type of analysis anticipated, the method of analysis shall be described. The likely tools used in conjunction with the analyses shall be named, including version numbers, if available.

2. Worst-Case Operating Modes and Conditions

The WCCA Plan shall contain a description of how the worst-case operating modes and conditions will be determined for use within the WCCA.

3. Personnel Resources

The WCCA Plan shall contain a description of the personnel resources that will be needed to execute the WCCA activity, including both analyst, as well as reviewer resources. Include such items as experience level, familiarity with tools, years on program, etc. If external analysis resources are to be procured, the company name and a brief description of their qualifications shall be provided.

4. Parts Characterization Resources

The manner in which parts characterization data is obtained and managed shall be described.

5. Model Validation

The WCCA Plan shall describe the sources of, as well as the types and fidelities of circuit and device models to be used in the analyses. Description shall be provided as to how models reflect EOL parameters and probability distributions, and how test data is used to validate part circuit and device models.

6. Testing

The manner in which device, breadboard, or engineering unit testing will be used to support the WCCA activity shall be described.

G. Schedule with Key Milestone Dates

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A.4 Parts Characterization and Database

A. A master database of parts parameters for WCCA purposes shall be developed and maintained. At a minimum, this database shall contain data relevant to a unit-level WCCA. Higher levels of organization, such as subsystem-level, program-level, or company-level, are acceptable, as long as it is possible to extract parts parameters for a unit-level or lower-level WCCA (i.e., module-level, card-level, etc.).

The database shall conform to the following requirements:

1. Organization
   a. The parts database shall be capable of sorting by generic part type (i.e., resistor, capacitor, BJT, power MOSFET, etc.), as well as particular sub-types (e.g., type RM resistors, CLR97 capacitors, etc.).
   b. A means should be provided to list all usage instances of a particular part type or part number.
2. Contents

For each particular part type (usually the DSCC part number), the database should contain the following information:

   a. the parameters relevant to WCCA
   b. initial tolerances of parameters or min/max values
   c. temperature coefficients of parameters
   d. aging or drift tolerances or min/max values of parameters
   e. radiation tolerances or min/max values of parameters (for total ionizing dose, dose rate, or displacement damage, as applicable)
   f. references or links to the sources of the data
   g. explanatory notes, where necessary
   h. Indication of whether the parameter is biased or random
3. Data Sources shall be per the requirements of Appendix 2.

B. The database shall be established as early as practicable in the WCCA process.

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A.5 WCCA Methodologies

A. General

1. For each separate circuit analysis, the results shall show the minimum, typical, and maximum values of each quantity of interest over End-of-Life (EOL) parameter variations.
2. When subject to Qualification or Protqual testing environments, WCCA shall be performed to ensure that no damage or malfunction to any circuit can occur as the result of the testing.

B. Extreme Value Analysis (EVA)

1. EVA shall be the default method for WCCA. If an analysis is performed using EVA, showing that the circuit meets requirements, no further analysis shall be necessary.
2. If a circuit does not meet a requirement using EVA, RSS techniques may be performed instead. Statistical analyses must be performed to an approved confidence interval/probability coverage, usually corresponding to a three-sigma or 99.73% probability of success.
3. Part Parameter Calculation for EVA

   The minimum and maximum values of a part parameter shall be calculated using algebraic summation.

   $$P(MIN) = P(NOM)(1-I-T-A-R)$$
   $$P(MAX) = P(NOM)(1+I+T+A+R)$$

   Where: P = Nominal parameter value at the nominal temperature
   I = Variation due to initial tolerance (%/100)
   T = Temperature variation = $TC*(T_{MAX} - T_{NOM})$ OR $TC*(T_{NOM} - T_{MIN})$
   A = Aging variation (% change /100) at EOL
   R = Radiation variation (% change / 100) at EOL

   Note: 1) in EVA, I, T, A, and R are considered to be positive values.

C. Monte Carlo Analysis (MC)

When Monte Carlo analysis is performed, the following information shall be provided:

- The list of parameters to be varied in the analysis
- The list of simulation conditions or environments (i.e., input voltage, loading, temperature range, etc.)
- A clearly-annotated simulation schematic.
- The probability distributions used for the parameters
- An example of how the probability distribution is implemented in the simulation software
- The number of simulation runs with statistical justification to meet the approved probability and confidence level.
- The histogram of the simulation output values for each quantity of interest.
- If possible, the sets of parameter values that produce the min and max values of the quantity of interest should be provided.

D. Root-Sum-Square (RSS) Analysis

1. When RSS analysis is performed, parameter variations shall be divided into biased and random terms. Only the random terms shall be RSS'ed; the biased terms shall be added:

$$WCmin = Nominal - \sum Negative\ Biases - \sqrt{\sum (Random\ Terms)^2}$$

$$WCmax = Nominal + \sum Positive\ Biases + \sqrt{\sum (Random\ Terms)^2}$$

2. Where significant cross-correlations exist between parameters, these shall be included in the RSS calculation.

E. Sensitivity Analysis

1. When using the sensitivity method for calculation of some function of multiple part parameters, the part parameter variations shall be calculated using EVA. The function (circuit performance) itself may be calculated using either EVA or RSS; however, RSS may only be used when there are three or more terms in the expression for the function. It is acceptable to use RSS either at the part parameter level or at the circuit level, but not both.
2. When using sensitivity analysis, the monotonicity of the perturbed variables shall be evaluated to ensure validity of the analysis.
3. When computer-aided circuit analysis software is used to generate sensitivities automatically, the operating point of the circuit shall be provided.

F. Combined Circuit Outputs

1. When two or more separate circuits contribute to some quantity of interest (for example, separate gain stages in a series chain, with overall gain as the quantity of interest) and that quantity of interest fails EVA, it is acceptable to use RSS as an alternative method, either at the part parameter level or at the circuit level, but not both.
2. RSS analysis shall only be used when there are three or more output quantities to be combined.

F. Analysis Tools

1. Manual Analysis
   a. Manual analysis, if used, shall be clear and well-annotated, so that the flow of reasoning is apparent to reviewers.
2. Circuit Simulation Software
3. Spreadsheets
   a. Formulas using cell references should be avoided for complex mathematical expressions. In Microsoft Excel, well-commented functions or subroutines written in Visual Basic for Applications (VBA), and using descriptive variable names instead of cell references, can be used instead to enhance clarity.

4. Mathematical Software

   a. Very complicated symbolic expressions should be avoided. If this is not possible, a second means of analysis should be used to ensure no mistakes have been made.

   b. Use of excessively long subscript notations should be avoided.

5. Custom Software

   a. Custom software, such as VBA routines, is acceptable if properly tested and documented.

G. Validation of Analysis Results

1. Peer Review – WCCA products shall be reviewed by knowledgeable peer reviewers prior to delivery.

2. Model Validation

   a. Simulation models of both circuits and devices shall be validated for the applications in which they are to be used.

3. Correlation with Test Data

   a. Breadboard or Engineering Model data should be used to augment the WCCA, especially for less commonly-used or more complex circuit types.

   b. For DC-DC converter models or for linear regulator circuits, phase/gain margins or output impedance shall be validated through testing of equivalent hardware prototypes at three or more sets of realistic operating points.

4. Two or More Methods

   a. When practicable, WCCA using one method should be augmented by a second method. For example, a simplified or detailed manual EVA analysis can be compared to SPICE simulation results.

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A.6 Worst-Case Conditions

WCCA shall be performed using conditions of worst-case part parameters and environments, per the following requirements.

A. Part Parameter Tolerances and Variations

1. Initial Tolerance Distribution

   The as-purchased initial percentage tolerance of an individual part or parameter, combined with specified environmental and handling factors, shall be considered as the absolute limit of initial variation for WCCA purposes. For example, the initial variation for a voltage reference is specified as ±0.5% across the specified operating temperature range and input voltage range. By contrast the limit of initial variation for a 1% 55342-type resistor might be ±1.55%, including the specified limit of ±0.20% for shift due to soldering, and ±0.35% from the specified temperature coefficient.

2. Temperature Effects

   a. Parameter variations due to temperature effects shall be included in the WCCA.

   b. Part temperature maxima and minima for WCCA purposes shall be coordinated with the thermal analysis or through demonstrably conservative assumptions.

3. Radiation Degradation

   a. Radiation effects on part parameters shall be included in the WCCA.

   b. Enhanced Low-Dose-Rate Sensitivity (ELDRS) data shall be included in the WCCA, for ELDRS-susceptible parts.

   c. Where applicable, prompt or dose-rate effects shall be included in the WCCA.

   d. Information on Single Event Transient, Upset, Burn-out, or Gate-Rupture (SET,SEU, SEB, or SEGR) effects on parts, as well as their associated rates or probability of occurrence, shall be considered in the WCCA, as practicable, to assure immunity of the design to upset or deleterious or damaging effects.

   e. Extrapolation of radiation degradation data for parts to higher-than-tested radiation levels shall not be permitted.

4. Radiation Design Margin

   WCCA shall be performed to show Radiation Design Margin (RDM) per program requirements. Shielding effects due to the spacecraft body, unit enclosures, or other shielding means may be included in the WCCA assumptions per program approved methodology.

5. Aging and Drift Mechanisms

   a. Variations of part parameters due to relevant aging and drift mechanisms shall be included in the WCCA.

6. Source of Data

   a. Part parameter variations of initial tolerance, temperature drift, aging effects, and radiation effects shall be per the relevant PMP standard or DSCC or DLA data sheet.

b. Test data may be used, in lieu of part parameter variations from PMP standards or DSCC/DLA data sheets, if valid rationale is provided.

c. see Section VI and Appendix 2 for detailed parts characterization requirements.

B. Applied Voltages

1. Bus Voltage

a. The WCCA shall consider spacecraft bus DC normal operating range, undervoltage operation and survival (essential bus equipment only), steady-state overvoltage, step-load positive- and negative-going transients, and fault-clearing positive- and negative-going spikes.

2. Power Converter Voltages

a. WCCA for circuits powered with secondary voltages from a power converter shall assume voltage ± tolerance from the power converter specification.

b. Positive- and negative-going transients due to worst-case step loads shall also be considered in WCCA for circuits powered with secondary voltages from a power converter.

c. Voltage-sequencing effects on circuits using multiple secondary voltages shall be considered in the WCCA.

d. Cross-regulation effects on power converter voltages shall be considered in the WCCA.

C. Loading Effects

WCCA for all types of circuits shall take into account effects due to intended loads and their time profiles, as well as relevant parasitic loads. DC, AC, periodic and aperiodic transient load types shall be considered. Worst case EOL load impedance and current shall be used. Interconnect impedances and load capacitances (including ESR effects) shall also be considered.

D. Operating Modes and States

1. WCCA shall take into account applicable operating modes and states, as well as any transitions between them. These may include, for example, steady-state, start-up, shutdown, standby, operate, etc.

2. WCCA for a given circuit may be limited to the mode or state that causes the most stressing operating conditions if a sound rationale is provided for why it is the most stressing.

E. Temperature Environment

1. The WCCA shall be performed to show full compliance with all requirements at EOL conditions over the acceptance temperature range for the unit under analysis, unless the qualification or protoqualification range is required by the program.

2. To demonstrate that no damage will be done by testing the unit over the Qualification or Protoqualification temperature range (whichever is applicable), the WCCA for the unit's power converter and other critical circuits whose malfunction could cause harm shall be evaluated using the applicable temperature range, with the aging and radiation tolerances set to zero (BOL assumption).

3. Cold-start analysis shall assume the low temperature of the qualification or protoqualification range.

F. Electromagnetic Compatibility

Conducted Emissions (CE) and Conducted Susceptibility (CS) requirements shall be considered for inclusion in the WCCA.

G. Wiring, Interconnects, Fusing

1. WCCA shall take into account the properties and effects of wiring and interconnects:
   a. DC voltage drop, when relevant.
   b. Temperature effect on DC resistance, including self-heating.
   c. High-frequency parasitic, when relevant.
   d. Coupling between wires or traces (capacitive or magnetic), including within wire harnesses or bundles, when relevant.
   e. Transmission-line effects, when relevant.
   f. Signal Integrity effects of a chain of PWB traces and interconnects (also external cables and connectors for interfaces)
   g. or wiring in the primary side of a power converter, current-carrying capability of wires and traces at 2X the current-protection level of the path.
   h. current-carrying capability of wires in a bundle at 2X the level of current protection of the path.
   i. Source and load impedances

H. Interfaces

1. WCCA for interfaces between units within a given subsystem shall be the responsibility of the subsystem provider.
2. WCCA for interfaces not contained within a subsystem shall be the responsibility of the prime contractor or systems integrator.
3. The WCCA for an interface shall validate the full end-to-end electrical design compatibility of the interface.
4. Test-Like-You-Fly validation of interfaces may be used to help validate models for their worst-case analyses.

I. Electrical Part Stress Analysis

1. Steady-state stresses (including repetitive stresses) shall be computed for each electronic part for the most unfavorable combination of realizable conditions, to determine compliance with applicable deratings as set forth in the applicable PMP requirements.
2. Aperiodic stresses due to transient conditions (on/off, line or load steps, mode changes, etc.) shall be computed for affected parts for the most unfavorable combination of realizable conditions. The effects of these stresses on part reliability shall be adjudicated by the PMPCB.

J. Calibration or Set-In-Test Considerations

1. WCCA may include rationale for omitting or reducing initial tolerance or other error terms when circuits are subject to calibration during operations.
2, WCCA may include rationale for omitting or reducing initial tolerance effects when Set-In-Test (SIT) resistors or other trim mechanisms are employed during the circuit build process.
3. The summary section of the WCCA report shall descriptively list each circuit function and part reference number where calibration and/or SIT mechanisms are assumed in the WCCA.

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A.7 Configuration Control

A. Each WCCA analysis shall contain a version and revision designation.

B. WCCA version and revision designation shall be traceable back to the specific hardware and specification configuration, by including in the WCCA:

   1. Schematic and assembly drawing numbers, including revision designators
   2. Hardware dash numbers of unit and subunits (down to Printed Wiring Assembly level)
   3. Engineering change orders (only the ones that resulted in a revision to the WCCA)
   4. All supplementary analysis and data package shall be retained along with the WCCA reports.

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A.8 Documentation and Other Deliverables (WCCA Data Package)

A. WCCA Report

A formal report(s) shall be provided to document the WCCA activity, containing the following information:

1. Title Page containing document number
2. Table of Contents (TOC)
   a. The TOC shall be hierarchically organized in a logical fashion to allow ease of navigation to sections of related subject matter.
   b. Each page number shown in the TOC shall contain a hyperlink to that page.
3. Table of Figures
4. Table of Tables
5. List of Compliance Documents (e.g., unit specification, PMP Standard, etc.)
6. List of Reference Documents
7. Configuration Control Information per VII.B
8. General Information, including
   - Background information
   - Global environmental conditions and other assumptions
   - List of circuits and parts where Select-In-Test and/or calibration is assumed in the WCCA.
   - List of parts and parameters for which lot-specific test data is used.
   - Other relevant information
9. Executive Summary of Results
   a. The Executive Summary shall contain a full listing of WCCA results and findings, organized logically by functional or physical element.
   b. Findings shall be grouped and ranked by severity or criticality.
10. Compliance Matrix
    a. The complete WCCA Compliance Matrix (WCM) described in III.D, which is to have been maintained and completed through the WCCA process, shall be included in the WCCA report.
    b. The WCM shall be presented in tabular form providing a mapping from all formal and informal requirements to the analysis identifier or identifiers that demonstrate compliance to the requirements.
11. Performance Analysis Section
    a. The Performance Analysis section shall consist of the individual circuit analyses, grouped and ordered per the WCCA Plan.
    b. Each separate analysis shall contain the following information:
       - Name of analysis

- Brief description circuit function and inputs/outputs
- Statement of what is being analyzed
- End-to-end schematic (full or equivalent)
  - with enough detail to understand the analysis
- Requirement(s) to be met
  - Formal specifications, ICD Spec or ICD
  - Local requirements
- Statement of Analysis Approach
- Assumptions
- Worst-case conditions
- Analysis, fully annotated
  - Software used, versions
  - Mathematical derivations, with explanations
  - Tables
  - Figures and plots
  - Monte Carlo histograms and output plots
- Results and findings, which include performance margins and non-compliances. Where practical, summarize the results in tabular or matrix form.

12. Electrical Stress Analysis Section
    a. Steady-state and transient stress analysis results shall be summarized in tabular form. The table shall include the military or manufacturer's rating, the derated rating, WC stress conditions with rationale, the nominal and maximum applied stress, the maximum stress margin ratio (applied maximum stress/Derated Stress). Also, provide references or links to detailed analysis,
    b. For each transient stress analysis, rationale for any deviations from steady-state deratings shall be provided.
    c. Stress calculations should be computed based on the qualification or protoqualification temperature range.
13. Parts Modeling Information
    a. A section of the WCCA Report shall contain documentation of the parts modeling methodology and database structure.
    b. Parts modeling information shall be organized and presented so as to allow reviewers rapid access to data and assumptions used in the analyses.
14. Circuit Model Documentation
    a. Thorough documentation shall be provided for circuit models that are not readily understandable by a reviewer.

b. For all models where detailed review of the model is not possible or permitted, thorough evidence of model validation and correlation with test data shall be provided.

c. The documentation for circuit models shall consist of the following:

- brief description of what the model does and how it works
- clear equivalent circuit diagrams for all levels of circuit hierarchy, including subcircuits, behavioral blocks, etc., where available.
- explanation of unusual symbols or nomenclature
- clear values for all parameters in all circuit elements
- clear values for supply voltages, stimulus sources, etc.
- derivation of or reference to a document describing the derivation of the model
- explanation of model use, where necessary for clarity
- explanation of how the model is adjusted to accommodate worst-case parameter values
- evidence of model validation

B. Report Medium

The report medium should be chosen to optimize the following during the review process:

1. Searchability
2. Use of hyperlinks for rapid navigation
3. Speed of scrolling or page turning
4. Ease of navigating from the analyses to the requirements, assumptions, worst-case conditions, parts modeling information, etc., and back

C. Supplemental Files

Computer files used during or in conjunction with the WCCA process are considered part of the WCCA and should be included in the delivery of WCCA products. Some examples of such files are as follows:

– Relevant schematics, specifications, and other formal engineering for the unit under analysis
– Circuit simulation files (e.g., schematic or netlists, sub-circuits, etc.)
– Auxiliary spreadsheets or math software files
– Engineering memos used by or referenced in the WCCA
– Test data
– Detailed parts characterization data per Appendix 2
– Part radiation test data and derivations of EOL design limits
– Command media documents

D. Tools – The computer tools necessary to run the associated WCCA analyses shall be retained in case the analysis needs to be revisited at a later date.

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A.9 Reviews and Reviewability

A. Internal Peer Review

Each WCCA report shall be subjected to a rigorous internal peer review process prior to delivery.

B. Criteria for Reviewability

It is assumed that peer or third-party WCCA reviewers will have the requisite skills in circuit design and analysis for the types of circuits they are reviewing.

The criteria for reviewability of a WCCA data package are as follows:

1. No prior knowledge of or exposure to the unit under analysis shall be required of the reviewers.
2. The WCCA data package shall be complete as practicable, requiring no additional outside information for a thorough review
3. The WCCA data package shall allow for assessment of all equations, procedures, logical steps, etc., by the reviewer, such that the reviewer does not have to independently derive or re-create any of these to be sure of their correctness.

C. Interim Reviews

A minimum of two interim, informal, technical meetings between the WCCA analysis team and the customer's independent reviewers shall be held during the WCCA analysis phase to assess the work in progress. Reviewers should be provided schematics and preliminary copies of the analyses beforehand, allowing enough time to formulate comments and questions for discussion at the meetings.

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A.10 Definitions and Supplemental information

Acronyms

AC	Alternating Current
ASIC	Application Specific Integrated Circuit
BOL	Beginning Of Life
CDR	Critical Design Review
CE	Conducted Emissions
CS	Conducted Susceptibility
DC	Direct Current
DID	Data Item Description
DLA	Defense Logistics Agency
DPA1	Destructive Physical Analysis
DSCC	Defense Supply Center Columbus (DLA Land and Maritime)
ELDRS	Enhanced Low Dose Rate Sensitivity
EOL	End Of Life
ESD	Electro-Static Discharge
EVA	Extreme Value Analysis
FPGA	Field-Programmable Gate Array
ICD	Interface Control Document
MAIW	Mission Assurance Improvement Workshop
MMIC	Monolithic Microwave Integrated Circuits
PDR	Preliminary Design Review
PMP	Parts, Materials, and Processes
PMPCB	Parts, Materials, and Processes Control Board
RSS	Root Sum Square
SCD	Specification Control Drawing
SDRL	Subcontractor Data Requirement List
SDRL	Supplier Data Requirements List
SEB	Single-Event Burn-out
SEE	Single Event Effects
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SEU	Single Event Upset
SIT	Select In Test
SMD	Standard Microcircuit Drawing
SOW	Statement of Work
SSO	Simultaneous Switching Outputs
TID	Total Ionizing Dose
TOC	Table Of Contents
VBA	Visual BASIC for Applications
WCCA	Worst Case Circuit Analysis
WCM	WCCA Compliance Matrix

Definitions

Beginning Of Life	Circuit conditions subject to initial tolerance and temperature effects only, with no aging or radiation effects.
Biased Terms	Parameter with a known direction of change in response to some condition.
Class A, B, C, D	Space mission classes, from highest reliability (e.g., high value government spacecraft) to lowest (experimental spacecraft). See DOD-HDBK-343 for more detail.
Derived requirement	A requirement that is inferred or transformed from a higher-level requirement.
End Of Life	Circuit conditions including initial tolerance and temperature effects, as well as aging and radiation parameter degradations.
Extreme Value Analysis	Computing the maximum and minimum values of a circuit's performance by using the most extreme combinations of part parameters and environment variables.
FMEA	Failure Modes and Effects Analysis. Also FMECA (C = Criticality). A Reliability and Systems Engineering tool for systematically evaluating failure modes in a system.
Gaussian Distribution	See Normal Distribution.
Initial Tolerance	The specified variability of a part parameter's value, at specified conditions, as delivered by a manufacturer.
Local requirement	A requirement that is not directly traceable to formal requirements other than "the circuit shall work." Typically they ensure acceptable circuit operating conditions, including good design practice constraints (adequate phase margin, etc.). For example, a processor card may generate a 1.0V power form with a voltage regulation requirement of 4% to comply with the FPGA's requirements; a different FPGA might support the formal requirements but require a 1.2V ±3% supply. The circuit may misbehave if the 4% tolerance is not maintained through life, so WCCA is appropriate.
Monte Carlo Analysis	A circuit analysis in which a spread of performance results is obtained by aggregating the results of many separate simulations, each with randomly selected part parameter and environment variations.
Normal Distribution	A continuous probability distribution with a bell-shaped probability distribution; same as Gaussian Distribution. Convenient and often-accurate representation of physical properties.
Part	E.g. resistor, capacitor, microcircuit, transformer.
PMP Standard	A source document containing data and methodologies for evaluating part stresses and parameter shifts. Example: MIL-STD-1547B.
Random Terms	Uncorrelated variables. If the probability distribution for each is Normal, then the Root-Sum-Square (RSS) method may be used to determine the overall standard deviation.
Uniform Distribution	A continuous probability distribution with flat probability distribution and abrupt endpoints.

Validation (model validation)	Showing that a model predicts behavior or performance with sufficient accuracy, typically by comparing simulation predictions against measured performance.

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A.11 Tailoring Guidance For Class B, C, or D Missions

WCCA provides mission assurance. For Class A systems, very little risk is tolerated. For other classes of systems, more risk is tolerated. However, where formal WCCA is not required, there are alternative means to gain as much mission assurance as possible. The following lists provide guidance to descoping WCCA requirements along with suggestions that may be done in lieu of formal WCCA, but that still provide design confidence at a lower level of effort.

Class B – All the requirements for Class A generally apply, but some reduction of scope or exceptions may be considered, as follows:

- Non-critical circuits may be omitted from WCCA. These would be circuits that could tolerate a degradation of accuracy due to a WCCA outage, such as telemetry circuits
  - Coordinate with FMECA to determine which circuits are considered critical
- The Radiation Design Margin R_{DM} could be decreased from 2 to 1.5 or even 1.0, especially for shorter-duration missions
- Application of radiation shielding considerations to give local total dose at part level could be done without customer concurrence
- May descope WCCA Plan; recommend retaining Interim Meetings
- More acceptance of RSS method rather than EVA
- If no EDU is to be built, consider more extensive testing of breadboards or other prototypes

Class C – Further descoping from Class B as follows:

- Formal parts stress analysis should still be required
- Formal performance WCCA required only for critical subsystems or functions
  - Power system
  - Primary payload
  - Critical hardware with little or no heritage
- Emphasize “do no harm” analyses on secondary payloads
- Perform less formal, internal WCCA process on non-critical hardware
- In lieu of radiation testing on parts
  - use familiar parts with good flight heritage
  - perform limited radiation testing on new or exotic parts
  - use existing radiation database resources
  - perform literature searches on parts and processes to find radiation test results
  - avoid COTS parts, but if used, perform some radiation testing using sufficient samples to determine EOL design limits
  - provide extra radiation “spot” shielding for parts whose performance cannot be assured

    - design in immunity to part SETs (e.g., filtering or current limiting)
- Use WCCA checklists and guidelines during design process – designers perform their own informal or "back of the envelope" WCCAs as they design
- Perceptive instrumentation and testing of breadboards and prototypes. Characterize waveforms to ensure transient stresses are within expected limits

Class D – No formal WCCA required, but should use good design practices

- Formal stress analysis not required
- Use WCCA checklists and guidelines during design process – designers perform their own informal or "back of the envelope" WCCAs as they design
- Perceptive instrumentation and testing of breadboards and prototypes. Characterize waveforms to ensure transient stresses are within expected limits
- Emphasize "do no harm" analyses and informal FMECAs
- Avoid parts with known radiation susceptibilities

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A.12 Example WCCA Compliance Matrix (WCM)

Populate in WCCA Plan	Populate in WCCA Plan	Populated in WCCA Plan	Populated in WCCA Plan	Blank OK for WCCA Plan	Blank OK for WCCA Plan	Blank OK for WCCA Plan	Blank OK for WCCA Plan	Blank OK for WCCA Plan	Populate in WCCA Plan	Populate in WCCA Plan (planning stage: preliminary organization of reports)	Populate in WCCA Plan	Optional Populate in WCCA Plan	Not Populated in WCCA Plan	Not Populated in WCCA Plan
Spec ID #; Spec	**Spec Value**	**Unit/Module**	**Requirements Docs**	**Predicted BOL**	**Predicted Nominal**	**Predicted EOL**	**Comply (Y/N)**	**Margin**	**WCCA Plan Analysis Approach**	**Evidence**	**Analyst**	**Notes**	**SME Review Comments**	**IPT Response**
ADC_2328 The DNL for all data channels of the ADC Unit shall be less than 2 LSB	< 2 LSB	ADC Unit	ADC Spec	< 1.4 LSB	0.8 LSB	< 1.8 LSB	Y	0.2 LSB	Apply statistical processing of Pre & Post TID test results of data channel ADCs (tested over temperature) apply setbacks to acceptance limits to guarantee 2 LSB at EOL, use power supply headroom tests with setbacks to verify power supply min/max has no impact on DNL.	DNL + TID Test Report (ADC Module Report 1228); Power Supply Headroom Test Report (ADC Module Report 1232)	C. Shannon	Example of a unit requirement which is analyzed at the unit level		
ADC_1522 Aux Biases shall transition from off to on within regulation in less than 0.10 second from receipt of command.	< 0.1 second	ADC Unit	ADC Spec	0.079 s	0.074 s	0.079 s	**Y**	0.021 s	Add results of Digital Interface Module timing and Aux Bias Module response.	Aux Bias Module Report 102	D. Boeuf	Example of a unit requirement which is flowed down to two modules		
3.3.3.2.8 Time from Spacewire Command receipt to delivery of SPIO Command	< 0.02 second	Digital I/O Module (DIM)	DIM Spec	0.009 s	0.009 s	0.009 s	**Y**	0.011s	Simulation of VHDL code to determine the processing latency between the SpaceWire command (Aux Enable) and the SPIO data transmitted.	DIM Module Report 8	S. Morse	Example of a module requirement derived from a unit requirement		
3.3.5.2.3 Process SPIO command and enable Aux Bias Outputs to within regulation.	< 0.08 second	Aux Bias Module (ABM)	Aux Bias Spec	0.07 s	0.065 s	0.07 s	**Y**	0.01s	Simulation of VHDL code to determine the processing latency between the SPIO data received and the required timeline to update the DACs. Add the analog settling time from SPICE simulation of Aux Bias drive circuits with worst-case load.	Aux Bias Module Report 107	D. Boeuf	Example of a module requirement derived from a unit requirement		

Notes:

EOL prediction: worst case throughout life, typically occurs at end of life. Primary output of WCCA analysis.
BOL prediction: worst case at beginning of life, before component aging occurs. Typically used when determining test limits.
Nominal prediction: 25C beginning of life, nominal inputs & outputs, component values at nominal values i.e. +/- 0% tolerance. Useful as sanity check for BOL & EOL computations, and expected value for DVT (Design Verification Testing).

Margin: EOL prediction vs. Specification

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Local Requirement Description	**Value**	**Unit/Module**	**Requirements Docs**	**Predicted BOL**	**Predicted Nominal**	**Predicted EOL**	**Comply (Y/N)**	**Margin**	**WCCA Analysis Approach**	**Evidence**	**Notes**	**Analyst**
Mandatory Digital												
Fanout												
IC "NC" (no connect)												
Tristated Inputs Floating												
Logic Compatibility: Static												
Logic Compatibility: Dynamic												
Noise Margin: Crosstalk												
Noise Margin: DC Levels including Common-Mode												
Common-Mode voltage range												
Metastability												
State Machine Analysis												
Timing Margin Analysis, include Margin parameters, PWB Dielectric variability, Rise & Fall times, Clock Skew												
Physical: signal Integrity												
Physical: Decoupling Analysis												
Physical: Power Integrity												
Power Supply Sequencing												
Test Point Current Limiting												
Power Supervisor IC used per datasheet / app notes												
SEE Single Event Effects: circuit designer and radiation engineer list and review the response of parts to SEE and the resulting circuit behavior, and why resulting circuit behavior is acceptable.												
Digital: as applicable												
One-shot margin analysis												
White Wire Analysis												
Interface Circuits as applicable												
Logic Compatibility: DC Levels, common-mode voltage range, impedances												
High Level Discretes: DC Levels, common-mode voltage range, impedances												
Cold Spare interfaces review: logic, sneak paths												
Analog Circuits as applicable												
Discrete Bipolar Transistor Beta												
Discrete Bipolar Transistor Collector-Base leakage												
Discrete MOSFET Vgs drive headroom												
Discrete MOSFET Vds headroom												
Spare Opamps, Integrated Circuit "NC" (No Connection) review												
Opamp output voltage headroom												
Opamp input common mode voltage range												
Opamp input differential voltage range / input current limiting												
Opamp output current capability												
Opamp stability with capacitive load												
Phase Margin for amplifier & regulator circuits using discrete drive transistors												

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Local Requirement Description	**Value**	**Unit/Module**	**Requirements Docs**	**Predicted BOL**	**Predicted Nominal**	**Predicted EOL**	**Comply (Y/N)**	**Margin**	**WCCA Analysis Approach**	**Evidence**	**Notes**	**Analyst**
Acceptable impact of input power inductance (intentional or parasitic) on stability of linear regulator circuits (LC circuit at drain/collector)												
Monolithic voltage regulators operating with recommended range of decoupling capacitors												
Monolithic voltage regulators operating with recommended protection diodes (typically for protection if input of regulator is shorted).												
Monolithic regulators operating with all control inputs properly biased												
Monolithic regulator input voltage headroom												
Voltage reference IC input decoupling per datasheet and application notes												
Voltage Reference IC output capacitive loading per datasheet and application notes												
Voltage Reference IC output current within specified limits and impact on regulation factored into worst case performance												
Comparator output current and output voltage capability												
Comparator input differential and common-mode voltage range												
Verify acceptable circuit behavior when comparator power is being ramped on/off (Vdd < comparator minimum requirement)												
Input Overvoltage/Undervoltage stress at data converter and opamp inputs.												
Charging Impedance for Tantalum Capacitors (surge current)												
Current Limiting on outputs – circuits with external exposure should survive shorts to ground												
Survive abrupt application or short of input power												
Power Integrity: adequate decoupling, acceptable IR drops												
Power Supply Application and Sequencing Analysis												
Test Point Current Limiting												
Sensitive Signal Routing												
SEE Single Event Effects: circuit designer and radiation engineer list and review the response of parts to SEE and the resulting circuit behavior, and why resulting circuit behavior is acceptable.												

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Local Requirement Description	**Value**	**Unit / Module**	**Requirements Docs**	**Predicted BOL**	**Predicted Nominal**	**Predicted EOL**	**Comply (Y/N)**	**Margin**	**WCCA Analysis Approach**	**Evidence**	**Notes**	**Analyst**
Mandatory Digital: Not Applicable												
Interface Circuits as applicable												
Logic Compatibility: DC Levels, common-mode voltage range, impedances												
High Level Discretes: DC Levels, common-mode voltage range, impedances												
Cold Spare interfaces review: logic, sneak paths												
Analog Circuits as applicable												
Discrete Bipolar Transistor Gain												
Discrete Bipolar Transistor Collector-Base leakage												
Discrete MOSFET Vgs drive headroom												
Charging Impedance for Tantalum Capacitors (surge current)												
Monolithic voltage regulators operating with recommended range of decoupling capacitors												
Monolithic voltage regulators operating with recommended protection diodes (typically for protection if input of regulator is shorted).												
Monolithic voltage regulators operating with all control inputs properly biased												

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Monolithic voltage regulators operating with sufficient input voltage headroom												
Phase Margin and Gain Margin for discrete regulator circuits												
Acceptable impact of source impedance (intentional or parasitic) on stability of regulator circuits												
Opamp output voltage headroom												
Opamp input common mode voltage range												
Opamp input differential voltage range / input current limiting												
Opamp output current capability												
Opamp stability with capacitive load												
Comparator output current and output voltage capability												
Comparator input differential voltage range												
Comparator circuit behavior when supply voltage is less than comparator spec												
PWM Controller IC Operation												
MOSFET Driver IC Operation												
Voltage Reference IC input decoupling												
Voltage Reference IC output capacitive loading												
Voltage Reference IC output current loading												
Survive abrupt application or short of input power												

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Local Requirement Description	**Value**	**Unit/Module**	**Requirements Docs**	**Predicted BOL**	**Predicted Nominal**	**Predicted EOL**	**Comply (Y/N)**	**Margin**	**WCCA Analysis Approach**	**Evidence**	**Analyst**	**Notes**
Digital Signal Trace Impedances		Backplane	n.a.								.	
Digital Signal Crosstalk		Backplane	n.a.								.	
D.C. Drop		Backplane	n.a.								.	
Isolation of sensitive signals		Backplane	n.a.								.	
Physical grounding configuration matches unit grounding diagram		Backplane	n.a.								.	
Logic Level Compatibility		Backplane I/O	n.a.								.	
Logic Level Compatibility		Unit I/O	n.a.								.	
Digital Signal Trace Impedances		Unit I/O	n.a.								.	

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